ESC-TR-2001-078

Quarterly Technical Report

Solid State Research

2002:1

Lincoln Laboratory

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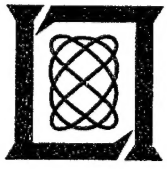

Prepared for the Department of the Air Force under Contract F19628-00-C-0002.

This report is based on studies performed at Lincoln Laboratory, a center for research operated by Massachusetts Institute of Technology. The work was sponsored by the Department of the Air Force under Contract F19628-00-C-0002.

The ESC Public Affairs Office has reviewed this report, and it is releasable to the National Technical Information Service, where it will be available to the general public, including foreign nationals.

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FOR THE COMMANDER

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Solid State Research

Quarterly Technical Report

1 November 2001— 31 January 2002

Issued 2 August 2002

Lexington Massachusetts

ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 November 2001 through 31 January 2002. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, DARPA, MDA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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INTRODUCTION

1. QUANTUM ELECTRONICS

Wavelength-beam-combining techniques have been investigated for increasing the brightness of several ytterbium fiber lasers, and power scaling has been demonstrated with a master oscillator–power amplifier configuration. Issues associated with increased power are discussed.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

A high-brightness semiconductor diode laser structure, which utilizes a slab-coupled optical waveguide region to achieve several potentially important advances in performance, has been experimentally demonstrated using a simple rib waveguide in an InGaAsP/InP quantum-well structure operating at 1.3-μm wavelength. These lasers operate in a large low-aspect-ratio lowest-order spatial mode that can be butt coupled to a single-mode fiber with high coupling efficiency.

3. SUBMICROMETER TECHNOLOGY

Deep-uv acid-catalyzed resists have been evaluated for use in mask making applications with electron beam exposure. These experiments revealed a chemical interaction between the photomask substrates and the resists that resulted in performance degradations, but these effects can be reduced by using a barrier layer between the resist and the chrome.

4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

Some methodologies and effects of cell freezing on the CANARY (Cellular Analysis and Notification of Antigen Risks and Yields) assay have been examined. A benefit of using cells that are frozen and recently thawed is that the photon output from these cells in response to agent is both stronger and more consistent.

5. ADVANCED IMAGING TECHNOLOGY

Simulated transient analysis has been used to analyze the electronic shutter switching characteristics for nanosecond time frame voltage pulses.These simulations show that the shutter is dynamically opened and closed in nanosecond times despite the fact that depletion-region formation and collapse take much longer times.

6. ANALOG DEVICE TECHNOLOGY

A fully integrated analog-to-digital converter (ADC) on a charge-coupled device (CCD) focal plane, along with all necessary control and clock circuitry and CCD gate drivers, has been designed. The simulated dynamic range is ~10.5 effective bits with pixel charge resolution of ~18 photoelectrons, the output

rate is 10 Mpixels/s, and the power dissipation of the ADC is ~10 mW with the entire chip including imager expected to dissipate ~25 mW.

7. ADVANCED SILICON TECHNOLOGY

A T-gate structure has been implemented in the fabrication of fully depleted silicon-on-insulator metal-oxide semiconductor field-effect transistors. The T-gate process is fully compatible with the standard CMOS, and the resulting reduction of gate resistance significantly improved the rf performance.

REPORTS ON SOLID STATE RESEARCH
1 NOVEMBER 2001 THROUGH 31 JANUARY 2002

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Controlled Contamination of Optics under 157-nm Laser Irradiation	T. M. Bloomstein V. Liberman S. T. Palmacci M. Rothschild	*Proc. SPIE* **4346** (Pt. 1), 685 (2001)
Periodically Poled $BaMgF_4$ for Ultraviolet Frequency Generation	S. C. Buchter T. Y. Fan V. Liberman J. J. Zayhowski M. Rothschild E. J. Mason* A. Cassanho* H. P. Jenssen* J. H. Burnett*	*Opt. Lett.* **26**, 1693 (2001)
High-Performance Fully-Depleted SOI RF CMOS	C. L. Chen S. J. Spector R. M. Blumgold* R. A. Neidhard* W. T. Beard* D-R.W. Yost J. M. Knecht C. K. Chen M. Fritze C. L. Cheny* J. A. Cook* P. W. Wyatt C. L. Keast	*IEEE Electron Device Lett.* **23**, 52 (2002)

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Detection and Identification of Donors in Hydride-Vapor-Phase Epitaxial GaN Layers	J. A. Freitas, Jr.* G. C. B. Bragda* W. J. Moore* S. K. Lee* K. Y. Lee* I. J. Song* R. J. Molnar P. Van Lierde*	*Phys. Status Solidi A* **188**, 457 (2001)
Magnetic Resonance Studies of Defects in GaN with Reduced Dislocation Densities	E. R. Glaser* J. A. Freitas, Jr.* G. C. Braga* W. E. Carlos* M. E. Twigg* A. E. Wickenden* D. D. Koleske* R. L. Henry* M. Leszczynski* I. Grzegory* T. Suski* S. Porowski* S. S. Park* K. Y. Lee* R. J. Molnar	*Physica B* **308–310**, 51 (2001)
Three-Dimensional Laser Radar with APD Arrays	R. M. Heinrichs B. F. Aull R. M. Marino D. G. Fouche A. K. McIntosh J. J. Zayhowski T. Stephens M. E. O'Brien M. A. Albota	*Proc. SPIE* **4377**, 106 (2001)

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Infrared Frequency Selective Surfaces Fabricated Using Optical Lithography and Phase-Shift Masks	S. J. Spector D. K. Astolfi S. P. Doran T. M. Lyszczarz	*J. Vac. Sci. Technol. B* **19**, 2757 (2001)
Effect of Substrate Orientation on Phase Separation in Epitaxial GaInAsSb	C. A. Wang D. R. Calawa C. J. Vineis	*J. Electron. Mater.* **30**, 1392 (2001)
Dry Etching of Amorphous-Si Gates for Deep Sub-100 nm Silicon-on-Insulator Complementary Metal-Oxide Semiconductor	D-R.W. Yost M. Fritze D. K. Astolfi V. Suntharalingam C. K. Chen S. G. Cann	*J. Vac. Sci. Technol. B* **20**, 191 (2002)

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Electronic Application of Superconducting Thin Films	D. E. Oates	Lincoln Laboratory Technical Seminar Series, Penn State University, State College, Pennsylvania, 5 November 2001
Orthogonal-Transfer CCD Technology for Large Mosaics	B. E. Burke	Large-Aperture Synoptic Survey Telescope Workshop, Tucson, Arizona, 5-6 November 2001
Future Prospects for Resolution-Enhanced Optical Lithography	M. Fritze	Lithography Strategies 2001, Austin, Texas, 7-9 November 2001

[†] Titles of presentations are listed for information only. No copies are available for distribution.

Wavelength Beam Combining of Mid-IR Semiconductor Lasers	A. K. Goyal A. Sanchez G. W. Turner T. Y. Fan Z. L. Liau M. J. Manfra P. J. Foti L. J. Missaggia P. W. O'Brien J. L. Daneu	Lasers and Electro-Optics Society Annual Meeting, San Diego, California, 12-15 November 2001
High-Performance, Aluminum-Free Optically-Pumped Mid-IR Semiconductor Lasers	A. K. Goyal G. W. Turner M. J. Manfra P. J. Foti P. W. O'Brien A. Sanchez	Lasers and Electro-Optics Society Annual Meeting, San Diego, California, 12-15 November 2001
Residual Phase-Noise Measurements of Actively Mode-Locked Fiber and Semiconductor Lasers	J. J. Hargreaves P. W. Juodawlkis J. J. Plant J. P. Donnelly J. C. Twichell F. Rana* M. E. Grein* R. J. Ram* E. P. Ippen*	Lasers and Electro-Optics Society Annual Meeting, San Diego, California, 12-15 November 2001
Relative Performance of Wide Bandgap Device Technology	Z. J. Lemnios R. A. Murphy J. C. Zolper*	Office of Naval Research Workshop, Marco Island, Florida, 12-16 November 2001
Magnetoelastic Effects of Iron-Group Ions in Exchange Fields	G. F. Dionne	Conference on Magnetism and Magnetism Materials, Seattle, Washington, 12-16 November 2001

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Analog Devices for Military Applications	D. E. Oates	Application of Superconductors in Electronics, Communication and Computing, Boston, Massachusetts, 15-16 November 2001
CANARY B-Cell Sensor for Rapid Identification of Pathogens	J. D. Harper M. A. Hollis	Center for Integration of Medicine and Innovative Technology Forum, Boston, Massachusetts, 19 November 2001
Electronic Application of Superconducting Thin Films	A. C. Anderson	Lincoln Laboratory Technical Seminar Series, University of Rhode Island, Kingston, Rhode Island, 21 November 2001
Nanodot Materials and Devices in PbSnSeTe-Based Quantum Dot Superlattices	T. C. Harman P. J. Taylor M. P. Walsh B. E. LaForge G. W. Turner	2001 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 26-30 November 2001
Gallium Vacancies as Acceptor Defects in *n*-Type GaN Layers Grown by Hydride Vapor Phase Epitaxy	J. Oila* J. Kivioja* V. Ranki* K. Saarinen* D. C. Look* R. J. Molnar Y. Park*	2001 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 26-30 November 2001
The Effect of Magnetic Field on the Anomalous Microwave Q of YBCO-on-MgO Resonators	S-H. Park* D. E. Oates J. Derov* G. Dresselhaus* M. S. Dresselhaus*	2001 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 26-30 November 2001

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Photoluminescence of Zn-Doped GaN	M. A. Reshchikov* D. Huang* H. Morkoç* R. J. Molnar	2001 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 26-30 November 2001
Photoluminescence Study of Deep-Level Defects in Undoped GaN	M. A. Reshchikov* H. Morkoç* S. S. Park* K. Y. Lee* R. J. Molnar	2001 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 26-30 November 2001
Lattice Misfit Strain Relaxation in PbTeSe/PbTe Quantum Dot Heterostructures	P. J. Taylor T. C. Harman M. P. Walsh B. E. LaForge R. L. Slattery G. W. Turner	2001 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 26-30 November 2001
Rapid Characterization of Free-Standing HVPE GaN Using Plan-View Transmission Electron Microscopy	P. J. Taylor R. J. Molnar J. M. Caissie A. H. Loomis L. J. Mahoney K. M. Molvar D. B. Hoyt G. W. Turner	2001 Fall Meeting of the Materials Research Society, Boston, Massachusetts, 26-30 November 2001
Contamination, Cleaning, and Performance of Optical Components	M. Rothschild	1st 157 nm Optical Lithography Symposium in Taiwan, Taipe, Taiwan, 26 November–2 December 2001
Optical Sampling for Analog-to-Digital Conversions	P. W. Juodawlkis J. J. Hargreaves R. D. Younger R. C. Williamson G. E. Betts J. C. Twichell	DARPA Advanced Signal Conversion Workshop, Washington, D.C., 27 November 2001

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Semi-insulating GaN for Device Applications	R. J. Molnar J. Caissie L. J. Mahoney K. M. Molvar M. Manfra* L. Pfeiffer* D. V. Lang* B. J. Skromme* K. Palle*	Office of Naval Research Sponsor Review, Boston, Massachusetts, 27 November 2001
Entangling Schrodinger's Cat: Superconductive Quantum Computation	K. Berggren	Mt. Holyoke College Seminar, South Hadley, Massachusetts, 29 November 2001
High-Fill-Factor, Burst-Rate Charge-Coupled Device	R. K. Reich D. M. O'Mara D. J. Young A. H. Loomis D. D. Rathman D. M. Craig S. A. Watson* M. D. Ulibarri* B. B. Kosicki	International Electron Devices Meeting, Washington, D.C., 2-5 December 2001
Lithium Niobate and Semiconductor Intensity Modulators	G. E. Betts	Optics and Quantum Electronics Seminar, Massachusetts Institute of Technology, Cambridge, Massachusetts, 5 December 2001
Controlled Contamination and Cleaning of Optics under 157 nm Laser Irradiation	T. M. Bloomstein S. T. Palmacci D. E. Hardy V. Liberman M. Rothschild	157 nm Data Review, Orlando, Florida, 10-13 December 2001

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Challenges of Long-Term Laser Durability Testing of Optical Coatings	V. Liberman M. Rothschild S. T. Palmacci N. N. Efremow J. H. C. Sedlacek A. Grenville*	157 nm Data Review, Orlando, Florida, 10-13 December 2001
Thin Inorganic Pellicles for 157 nm Lithography	M. Switkes P. W. O'Brien M. Rothschild	157 nm Data Review, Orlando, Florida, 10-13 December 2001
Immersion Lithography at 157 nm	M. Switkes M. Rothschild	157 nm Data Review, Orlando, Florida, 10-13 December 2001
An Optically Sampled Wideband Digital Receiver	P. W. Juodawlkis J. J. Hargreaves R. D. Younger G. W. Titi J. C. Twichell	2001 International Topical Meeting on Microwave Photonics, Long Beach, California, 7-9 January 2002
Optically-Pumped Mid-IR Lasers Based on Integrated Absorber Designs	G. W. Turner A. K. Goyal M. J. Manfra P. J. Foti A. Sanchez	SPIE Photonics West, San Jose, California, 19-25 January 2002
High-Performance CCD Imagers for Low-Light-Level Applications	B. B. Kosicki	Lincoln Laboratory Technical Seminar Series, Boston University, Boston, Massachusetts, 25 January 2002

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ADVANCED SILICON TECHNOLOGY

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1. QUANTUM ELECTRONICS

1.1 WAVELENGTH BEAM COMBINING OF YTTERBIUM FIBER LASERS IN A MASTER OSCILLATOR–POWER AMPLIFIER CONFIGURATION

Interest in combining large numbers of relatively low power lasers, to produce much more powerful high-brightness laser beams, is increasing. Coherent combining and wavelength (spectral) combining [1]–[3] are the two main approaches being studied. We have been concentrating on wavelength beam combining with fiber lasers and have previously demonstrated this concept at low power. Here we discuss recent work to extend this idea to a master oscillator–power amplifier (MOPA) configuration by adding a power amplification stage to each oscillator fiber and demonstrating recombination at higher powers. The conceptual layout is illustrated in Figure 1-1. Each fiber laser oscillates at a unique wavelength defined by the intracavity grating and the transform lens. The common arm between the grating and the high reflector contains spatially overlapped beams from each of the oscillator fibers. A fraction of the power is extracted from each array element with a fiber coupler to seed individual power amplifiers, each operating at a different wavelength. The amplified beams are then combined with a grating identical to the one in the oscillator cavities.

It is important that the power amplifiers are operated in a continuous-wave mode since pulses would cause catastrophic damage, and this is the advantage of a MOPA configuration for going to high power since the stages controlling spectral and temporal characteristics are separated from the power production stages. Pulsing behavior in Yb fiber oscillators has been studied by others [4] and observed by us. The pulsing has been attributed mainly to stimulated Brillouin effects, which are power dependent and therefore easier to suppress in a low-power cavity.

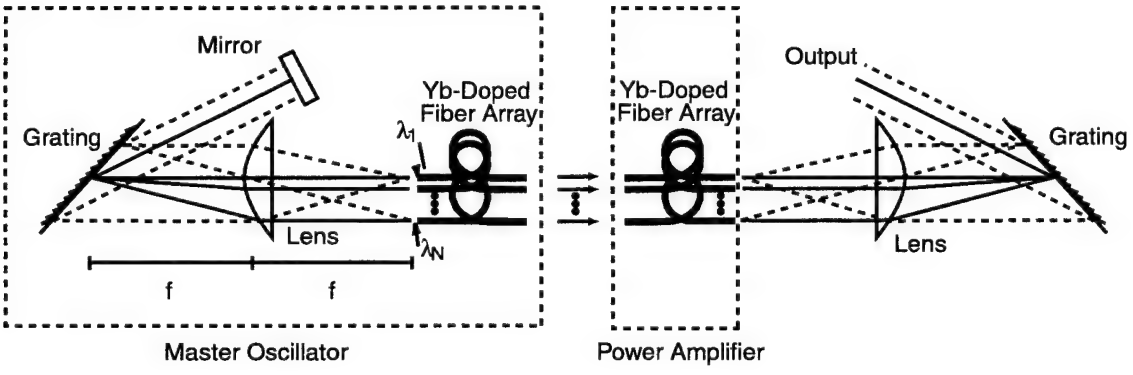

Figure 1-1. Conceptual layout of master oscillator–power amplifier configuration in which each fiber in the master oscillator operates at a unique frequency determined by the grating. Part of the light from each oscillator fiber is coupled into its own amplifier, and the amplifier outputs are recombined with an identical grating.

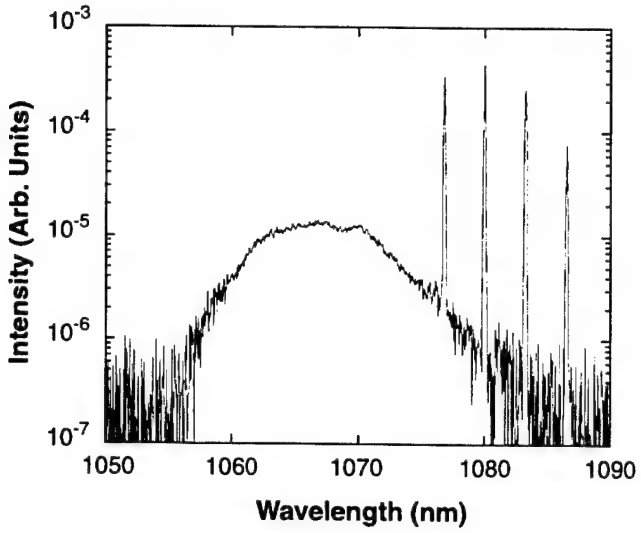

Figure 1-2. Spectrum of amplified beams. The fiber oscillators each have ~0.5-Å bandwidth, and here they are tuned away from the gain peak of the amplifier, which is evident by the amplified spontaneous emission peak at 1064 nm.

The spectral content of the amplified beams is shown in Figure 1-2. The amplified spontaneous emission of the amplifier here contains about 10% of the total energy, which can be reduced by tuning the oscillator fibers to overlap the gain peak of the amplifiers. Beam profiles have also been measured along with their respective M^2 values. It is found that when combining four fiber lasers the combined beam quality is nearly equal to the beam quality of individual laser elements. Figure 1-3 shows the beam diameters in the dispersion plane as a function of position as the beam goes through the focus of a 1-m lens. In our initial experiments, for low powers up to ~300 mW per fiber the combined beam profile M^2 value is equal to that of the individual laser elements within the measurement error. As the power is increased to ~1 W per fiber the beam profile worsens because of heating of the grating. The grating used for these measurements has an aluminum coating over a Pyrex substrate and a first-order diffraction efficiency of 65% (polarization averaged). Replacing this grating with one having a gold coating over a Zerodur substrate (72% polarization-averaged efficiency) has allowed the beam quality to be maintained at higher powers because of lower absorption of the gold vs aluminum and improved thermal properties of Zerodur vs Pyrex. Figure 1-4 shows the combined profile with 1.5 W per fiber and an M^2 value of 1.40 for the combined beams, which is equal to the M^2 values of the individual fibers. The overall improvement of M^2 from Figure 1-3 to Figure 1-4 reflects the improved grating characteristics as well as the removal of a hard edge that was lightly clipping the beam.

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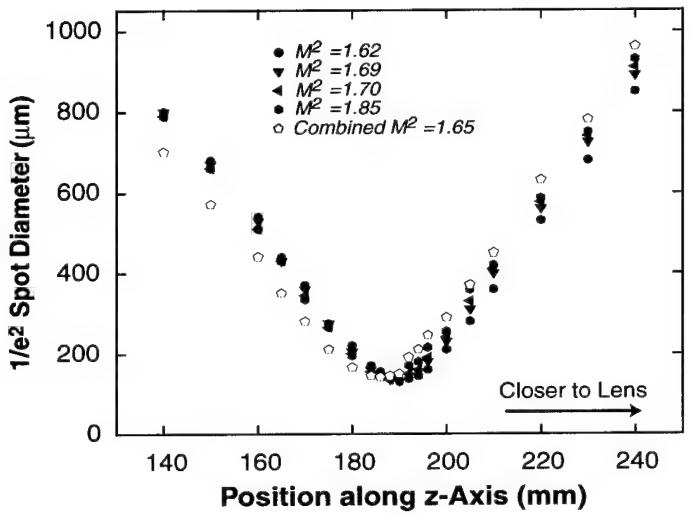

Figure 1-3. Dispersion-plane beam profile measurements comparing individual laser elements with the recombined beam. An aluminum-coated grating on a Pyrex substrate was used with a combined power of 1.3 W incident on the grating.

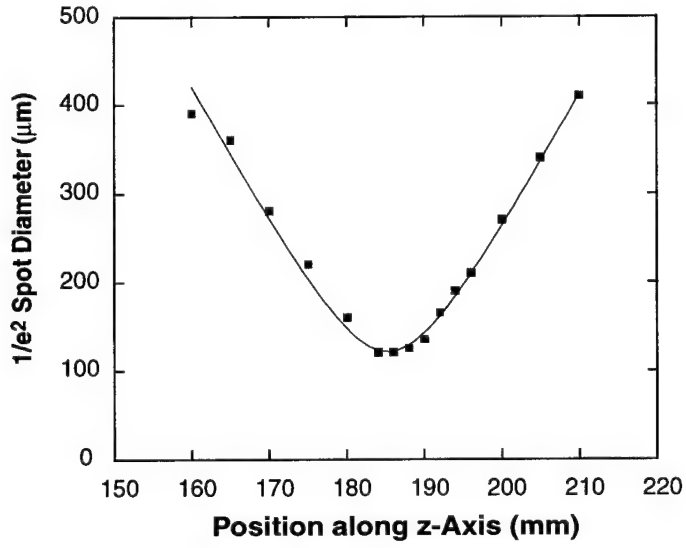

Figure 1-4. Dispersion-plane beam profile of four combined laser elements using a gold-coated grating on a Zerodur substrate. Combined power on the grating is 5.5 W with a curve-fit M^2 value of 1.40.

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2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 SLAB-COUPLED 1.3-μm SEMICONDUCTOR LASER WITH SINGLE-SPATIAL LARGE-DIAMETER MODE

Rib (ridge) waveguides are routinely used to control the mode profile in both active and passive semiconductor waveguides. Marcatili [1] showed, using a coupled-mode analysis between the rib region and the slab region, that the number of modes supported by a passive rib guide depends on the geometry of the rib structure and not on its actual dimensions. That is, the number of modes the rib structure will support depends only on the ratios *T/H* and *T/W*, where *T*, *H*, and *W* are effective dimensions of the guide. These are obtained by increasing the actual slab thickness *t*, rib height *h*, and rib width *w*, shown in Figure 2-1, by the field decay lengths in the adjacent cladding regions. The slab region acts as a mode filter to remove higher-order spatial modes. From a coupled-mode perspective, this filtering occurs because of coupling of the higher-order modes to the continuum of slab modes which then radiate energy laterally. In theory, therefore, it is possible to make a lossless single-mode guide of arbitrarily large dimensions. More precise analyses [2]–[3] showed that the cutoff for higher-order modes depends somewhat on the actual guide dimensions but, in general, supported Marcatili's results.

For lasers, a fundamental issue is whether enough gain can be selectively added to the rib region of a large rib guide so that the lowest-order mode reaches threshold without causing sufficient gain guiding that a higher-order mode becomes confined to the rib and attains a lower threshold than the desired mode. Since the real-index lateral confinement is small in a large rib guide, the gain in the rib region must also be small

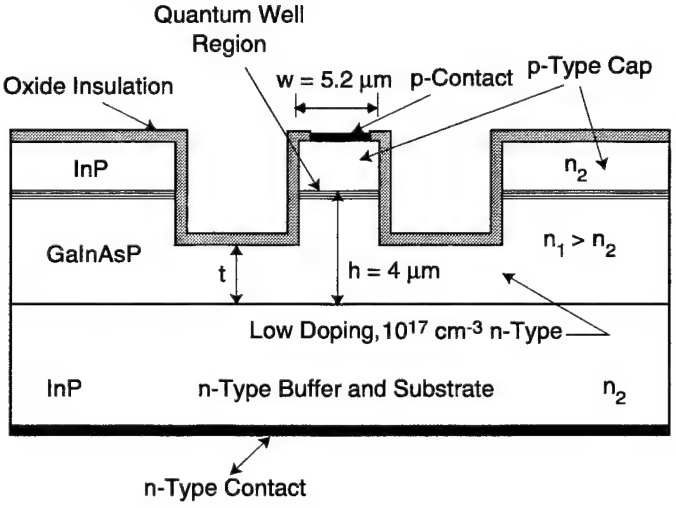

Figure 2-1. Proof-of-concept slab-coupled optical waveguide laser (SCOWL) structure.

to maintain the mode-filtering properties of the slab region. Hence, the losses in the guide due to free-carrier and other parasitic effects must be kept very small. Now, with the development of quantum-well regions with extremely small transparency-current densities that can be placed in large, otherwise passive waveguides, such structures are possible. The acronym we propose for these structures is SCOWL, from slab-coupled optical waveguide laser. SCOWLs promise high power and high brightness with large near-circular modes. The large mode size reduces the power density at the facet and permits butt coupling (no lenses) to a single-mode fiber with high coupling efficiency. Low parasitic loss also permits very long devices, making it easier to handle power dissipation without thermal waveguiding. Here, we present initial modeling and experimental results on a 1.3-μm InGaAsP/InP proof-of-concept SCOWL device.

The structure design was chosen for its relative simplicity and ease of fabrication. It also employs quantum-well gain regions and InGaAsP layers that have been used in our more conventional laser structures and therefore are well documented [4]–[5]. This device, illustrated in Figure 2-1, looks very similar to a ridge laser device except that the ridge is etched into the waveguide layer forming the rib region. The thickness of the waveguide layer is also much larger than used in standard single-mode lasers, and the height and width of the rib region are larger and nearly equal. The multiple quantum well (MQW) gain region was placed on top of the waveguide to avoid having a waveguide inside a waveguide, i.e., if this region is placed deeper within the waveguide, the lowest-order mode can become localized around the MQW region. The wafer used for the SCOWL device was grown by organometallic vapor-phase epitaxy. In order of growth on a (100) n^+-InP substrate, the structure consists of a 1.2-μm-thick n-InP cladding layer graded from $n \cong 1 \times 10^{18}$ to 5×10^{16} cm^{-3}, a 3.9-μm-thick latticed-matched n-InGaAsP (λ_g = 1.03 μm) quaternary waveguide layer, the MQW gain region which was not intentionally doped, a 1.5-μm-thick p-InP cladding layer graded from $p \cong 2 \times 10^{17}$ to 1×10^{18} cm^{-3} and a p^+-$In_{0.53}$ $Ga_{0.47}$ As contact layer. The doping in the n-type quaternary waveguide layer was ~5×10^{16} cm^{-3}, which was chosen as a compromise between free-carrier loss and series resistance. The MQW gain region consisted of five 8-nm-thick InGaAsP quantum wells under ≅1% biaxial compression, 10-nm-thick InGaAsP (λ_g = 1.09 μm) barriers, and 25-nm-thick bounding layers of the same composition. The bounding layer thickness was chosen to provide the desired confinement factor for the lowest-order mode.

Broad-area lasers fabricated in this material lased in the fourth-order transverse (perpendicular to layers) mode, as indicated by the agreement between the observed and calculated far-field pattern of the fourth mode, shown in Figures 2-2(a) and 2-2(b), respectively. The broad-area devices can support five slab modes, of which the third and fourth have the highest confinement factors. Therefore, the broad-area lasing mode should be either the third or fourth, depending on the relative values of their facet reflectivities. Measurements of threshold and quantum efficiency vs length indicate that the transparency current density and loss for the fourth-order mode are about 300 A/cm^2 and 1.85 cm^{-1}, respectively. In the etched SCOWL structure the loss of the higher-order modes increases significantly owing to lateral coupling to the slab, and fundamental-mode operation becomes possible.

A complex-index-mode solver was used to model the etched SCOWL and determine appropriate etch depths and rib widths for single-mode operation. To perform these calculations, an artificial boundary

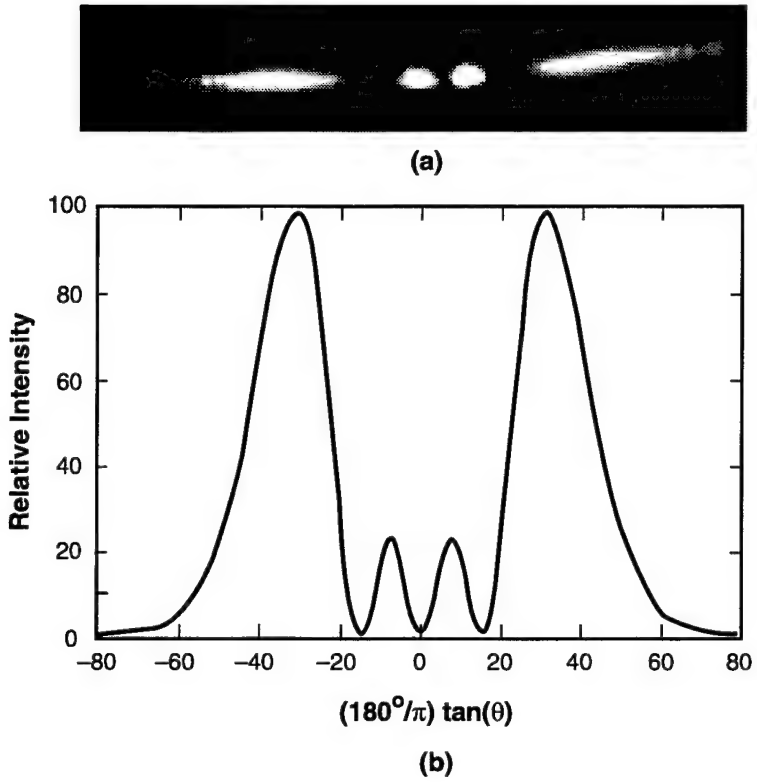

Figure 2-2. (a) Observed and (b) calculated far-field pattern of broad-area lasers (no rib etch) fabricated in InGaAsP material from which SCOWL lasers were fabricated.

was placed around the rib structure. This boundary was placed sufficiently far away that results were not affected significantly by the boundary placement. Real and imaginary parts of the refractive index were assigned to each layer. Gain was assigned to the quantum wells in the rib region while loss was assigned to the wells in the outer regions, as seen in Figure 2-1. Loss was assigned to all the other layers based on estimates of their free-carrier loss. Because of the artificial boundary, radiation modes are discretized. The results of one such calculation are shown in Figure 2-3, which plots the real and imaginary part of the modal index (components of the complex propagation constant divided by $k_o=2\pi/\lambda$, where λ is the wavelength) of each mode. Only quasi-TE modes were considered since the quantum wells are compressively strained. For the parameters chosen, only the desired lowest-order SCOWL mode has net gain (negative values of the imaginary part of the modal index) at laser threshold.

The devices were fabricated using a Ti etch mask and a combination of both CH_4/H_2 reactive ion etching and short chemical wet etches. Rib widths w of 5.2 μm and remaining waveguide thickness t in the slab region of 3.2 μm were chosen based on the mode calculations. The etched grooves, seen in Figure 2-1,

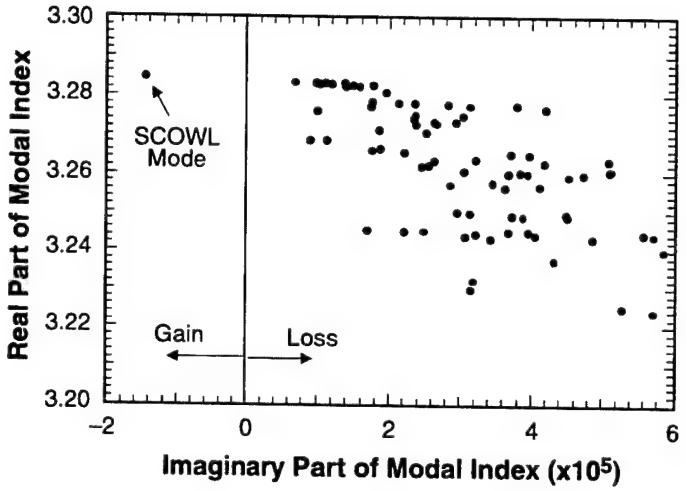

Figure 2-3. Results of one complex-index modal calculation that was used to determine the appropriate rib width and etch depth for single-mode SCOWL operation.

were 100 μm wide. The unetched field regions were retained, not only to increase the losses for higher-order modes, but also to facilitate junction-side-down mounting. The unetched field regions are sufficiently removed spatially from the lowest-order mode that they have no effect on it. After etching, the SCOWL wafer was coated with SiO_2, and standard contact and thinning procedures were used to complete the fabrication.

The near-field and far-field patterns of a typical 7.7-mm-long SCOWL device with uncoated facets are shown in Figure 2-4, which clearly indicates operation in the lowest-order fundamental mode. The near-field intensity pattern is about 4.0×2.2 μm while the far-field pattern is about $8 \times 18°$. These values agree with values calculated using the mode solver. All of the devices tested with uncoated facets, including devices as short as 4 mm (the shortest length tested), operated in the lowest-order fundamental SCOWL mode. Several devices were mounted junction side up to a Cu heatsink using In solder. Contact to the top (rib side) was made via wire bonds. Junction-side-up mounting was employed with these initial devices to avoid shorting problems associated with using In solder on junction-side-down InP devices. Devices 7.7 mm in length with uncoated facets had threshold currents I_{th} of ~0.5 A and initial differential quantum efficiencies per facet η_d of about 30% for both pulsed (5-μS pulses) and cw measurements. These quantum efficiencies are extremely high for lasers of this length and correspond to a modal loss of 1 cm^{-1}. The cw output power per facet of a typical device is shown in Figure 2-5. This device had >0.2 W/facet at 1.5 A and 0.3 W/facet at 2.3 A. The decrease in efficiency with increasing power is due, at least in part, to heating because of junction-side-up mounting. The small kinks observed at high power (which were not observed on all devices) are not well understood but, since the mode remained stable over the entire current range, are believed to be due to small asymmetrical changes in the power distribution along the length of

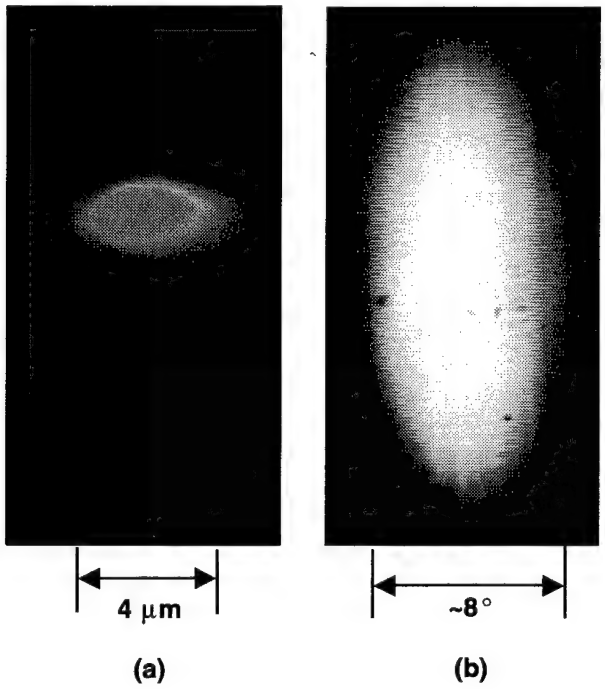

Figure 2-4. (a) Near-field and (b) far-field pattern of completed SCOWL device. The device is clearly lasing in the desired lowest-order SCOWL mode.

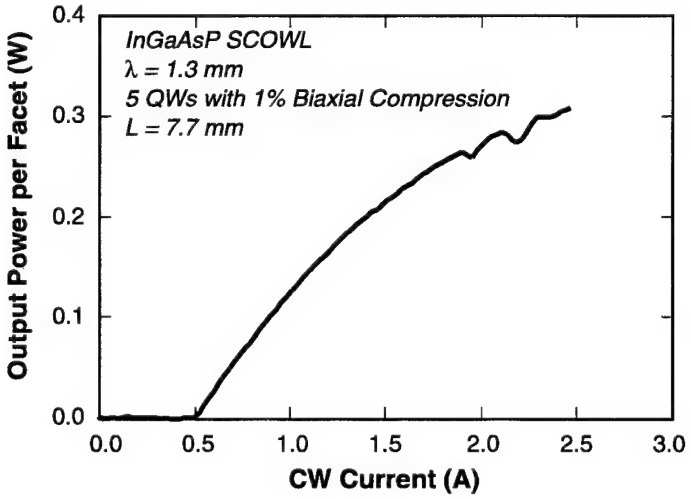

Figure 2-5. Continuous-wave output power from one facet of 7.7-mm-long SCOWL device with uncoated facets.

the device. Possible causes are nonuniform current injection and/or nonuniform heating. Results on devices taken from the same fabrication were consistent, with I_{th} ranging from about 0.5 to 0.52 A and η_d varying between 27 and 31% per facet. Adjacent devices had essentially identical characteristics.

For cw operation of a device at 2 A, >80% of the output power from one of the facets was butt coupled into a single-mode fiber with a mode diameter of 6.2 μm. This coupling efficiency is in fairly good agreement with a coupling efficiency of 86% calculated using the overlap between the theoretical mode profiles of the fiber and the SCOWL device. The overlap calculations also show that coupling efficiencies greater than 80% should be possible with fiber misalignments of +1 μm in either direction, because of the large mode size of the SCOWL device.

Thus, a high-brightness semiconductor diode laser concept utilizing a slab-coupled optical waveguide region to achieve several important advances in performance has been proposed, modeled, and demonstrated in a simple InGaAsP/InP MQW structure operating at 1.3-μm wavelength. The device is capable of single-spatial-mode operation with a single-lobed, large-area, low-aspect-ratio beam that is easily butt coupled to a single-mode fiber with high coupling efficiency. On these initial devices, 0.3 W/facet (0.6-W total power) was obtained, 80% of which could be butt coupled into a single-mode fiber. It is expected that the type of structure used for this first SCOWL device will be followed by many variations with significantly better performance. It should also be recognized that the SCOWL concept should be applicable to a wide variety of semiconductor material systems and wavelengths of interest.

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3. SUBMICROMETER TECHNOLOGY

3.1 USE OF ACID-CATALYZED RESISTS WITH ELECTRON BEAM EXPOSURE FOR MASK MAKING

The aggressive scaling in critical dimensions for integrated circuit manufacturing, coupled with the increasing use of subresolution features in optical proximity correction (OPC), dictates that by 2003 maskwriters will need electron beam resists capable of printing 100-nm OPC features on 280-nm design rule masks (70-nm features on the wafer) [1]. The low volume of e-beam resists used for maskwriters, estimated at less than 1000 gallons per year worldwide, has acted as a disincentive to resist manufacturers to develop or even evaluate resists for this application. To address this problem, under a cooperative research and development agreement with SEMATECH, we have been evaluating commercial deep-uv resists for use in e-beam mask making applications.

Chemically amplified (CA) resists, typically used in deep-uv lithography, are a potential way to improve e-beam mask making capabilities [2] for the 130-nm generation and beyond. This class of photoresist achieves high exposure sensitivity by using a two-step process. First, optical or electron beam exposure causes the generation of an acid; then during the post-exposure bake (PEB) this acid initiates a catalytic deprotection chain reaction that transforms the resist, making the exposed regions soluble in an aqueous base solution.

In this study, all e-beam exposures were made with a JEOL JBX-6000FS e-beam tool operating at 50 kV with a beam width of 20 nm and a pitch of 25 nm. The resolution test pattern contains feature sizes from 100 to 400 nm exposed at various doses used to determine dose to size, exposure latitude, and linearity. Dense structures with a 1:1 line-to-space ratio and isolated line structures with a 3:1 ratio are included in the test pattern. A total of 18 die are written on the wafer, arrayed in a horizontal line with the patterns stepped out every 300 μm. The pattern has proximity effect compensation features arrayed in the vertical direction between test structures.

Two different types of substrates were used: 6-in. silicon wafers and 6-in. synthetic quartz wafers coated with 105 nm of antireflective (AR3) chrome supplied by Hoya. The quartz wafers are similar to standard quartz photomasks, but they can be processed with a conventional automated coat/develop wafer track. The AR3 chrome is a proprietary inorganic antireflection coating (ARC) typically used on photomasks.

We studied five different commercially available CA resists. A list of suppliers and resists is presented in Table 3-1. All resists, except where noted, were coated to approximately 400 nm by spin casting from 2000 to 4000 rpm. The resist post-apply bake (PAB) and PEB were performed on a hot plate and varied according to supplier recommendations. Development was by single puddle with Shipley LDD-26W.

TABLE 3-1

Resists and Process Conditions Employed for Evaluating Substrate Sensitivity

Company	Resist	PAB Conditions	PEB Conditions	Develop Time
IBM	KRS-XE	100°C/90 s	25°C/30 min	60 s
Shipley	XP-9947W	140°C/90 s	130°C/90 s	60 s
TOK	OBER-CAP209-EL	150°C/90 s	130°C/90 s	60 s
JSR	TEBM 840	130°C/90 s	130°C/90 s	60 s
Nippon Zeon	ZCA-201	130°C/90 s	130°C/90 s	60 s

Initial screening of resists was performed on AR3 chrome coated synthetic quartz wafers from Hoya. An issue with substrate footing was observed that appeared to limit resist resolution and negatively impact the resist profiles. The lack of complete resist clearing between features is very reminiscent of footing behavior that was previously observed with CA resists on SiON substrates [3],[4]. This behavior can arise because of acid diffusion out of the resist and into the AR3 film or the diffusion of base contaminants from the AR3 film into the resist. In either case, acid loss at the resist-substrate interface leads to reduced resist deprotection. The reduced deprotection will lead to incomplete resist dissolution and will manifest itself as either resist footing between features or reduced resolution caused by incomplete development.

It is important to determine how general the incompatibility between CA resists and AR3 chrome is, and what processing or substrate preparation steps can be performed to eliminate this incompatibility. The resolution and resist profiles of the five test resists were determined on three different substrates. The substrates were Hoya AR3 chrome coated synthetic quartz wafers, hexamethyldisilazane vapor-primed silicon wafers, and Shipley AR3 organic antireflection layer coated on Hoya AR3 chrome wafers. The last substrate employs Shipley AR3 as an organic interlayer between the resist and the AR3 chrome. The Shipley AR3 was coated to a 65-nm thickness, followed by a PAB at 215°C for 60 s. It must be noted that Shipley AR3 is an organic ARC that unfortunately has the same name as Hoya AR3 inorganic ARC.

The five test resists were exposed with our resolution pattern, which consisted of dense lines from 400 nm down to 100 nm, and processed with the suppliers' recommended conditions. The processing conditions for each of the five resists are listed in Table 3-1. The exposure dose that gave 300-nm dense lines closest to their nominal linewidth was selected as the resist sensitivity or sizing dose

TABLE 3-2

Summary of Resist Resolution and Substrate Sensitivity on Different Resist Substrates

Resist	Sensitivity ($\mu C/cm^2$)	Resolution (nm) and Footing (Color)		
		Silicon	AR3 Chrome	AR3 Organic
KRS-XE	12.0	150[a]	150[c]	150[a]
XP-9947W	12.0	100[a]	150[a]	150[a]
OBER-CAP209-EL	2.8	150[a]	300[c]	150[a]
TEBM 840	9.8	150[a]	150[b]	150[a]
ZCA-201	6.6	200[a]	150[b]	300[c]

[a] No resist footing.
[b] Moderate footing.
[c] Severe footing.

E_{size}. All test structures at the E_{size} were cross sectioned and imaged by scanning electron micrography (SEM). The SEM images for each resist and substrate combination are presented in Figures 3-1 through 3-5. The resolution for each resist was determined by noting the minimum resolved feature at the E_{size}. In addition, the amount of resist footing was estimated and characterized as either none, moderate, or severe. The sizing dose, resolution, and amount of footing are summarized in Table 3-2.

None of the five test resists exhibited footing on silicon wafers and only ZCA-201 failed to resolve 150-nm dense lines. The silicon substrate thus can be used to compare the effects of acid loss of other substrates on the performance of the CA resists. The Shipley XP-9947W was the only resist to not suffer some degree of resist footing on AR3 chrome or the AR3 organic layer. The selection of moderate or severe footing is arbitrary, and SEM images of all resists and substrates are included in Figures 3-1 through 3-5 for visual comparison. Generally, if the resist has a thin undissolved film between clearly defined images, the resist was rated as having moderate footing, while a thicker undissolved film between images was rated as severe footing. The four other resists tested all exhibited either a moderate or severe amount of footing on AR3 chrome. Of these four resists, the KRS-XE and OBER-CAP209-EL had severe footing and the TEBM 840 and ZCA-201 had moderate footing. Only ZCA-201 had footing when the AR3 chrome was coated with a protective interlayer of AR3 organic film. The fact that ZCA-201 exhibited footing and had

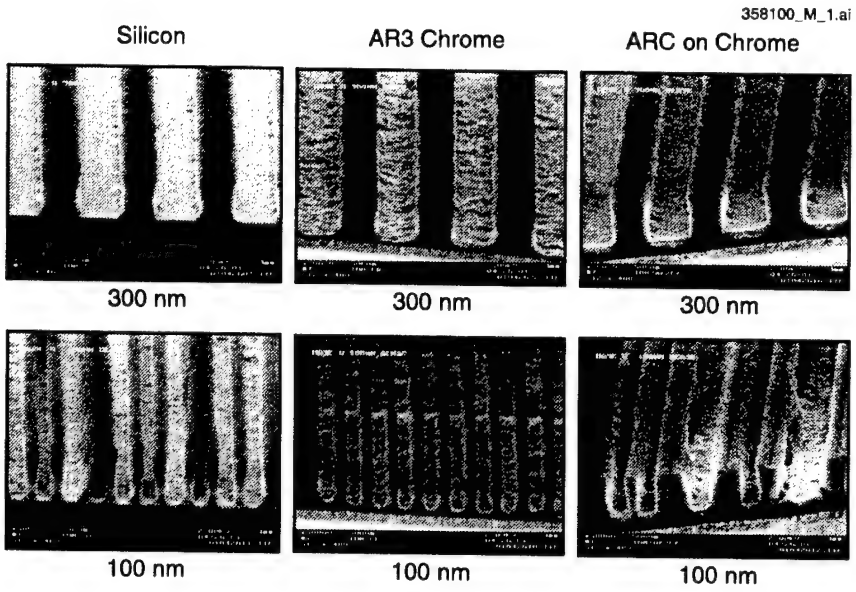

Figure 3-1. Imaging of 100- and 300-nm dense lines at 12 μC/cm^2 on KRS-XE on silicon, AR3 chrome, and organic antireflective coating (ARC) on AR3. Substrate sensitivity, manifest as incomplete development on AR3 chrome, is not present on silicon or ARC.

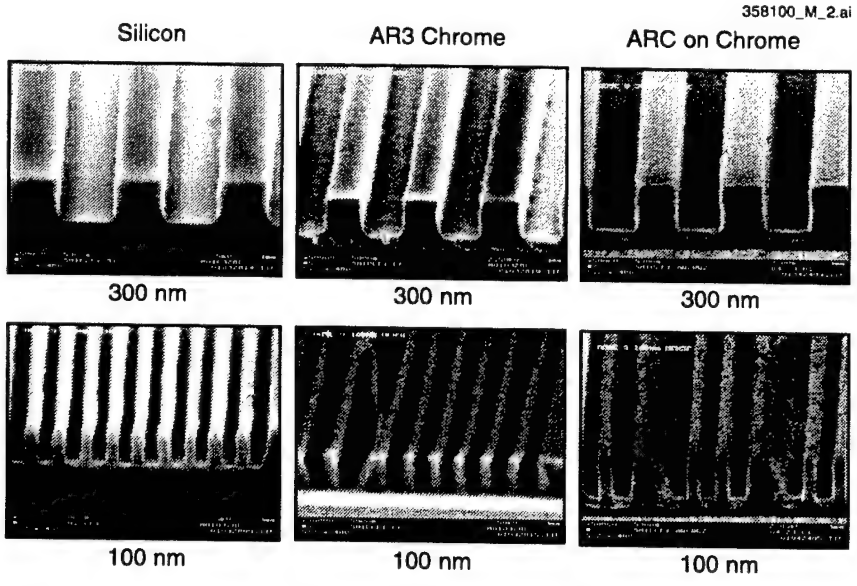

Figure 3-2. Imaging of 100- and 300-nm dense lines at 12 μC/cm^2 on XP-9947W on silicon, AR3 chrome, and organic ARC on AR3. Substrate sensitivity, manifest as incomplete development, is not present on AR3 chrome, silicon, or ARC.

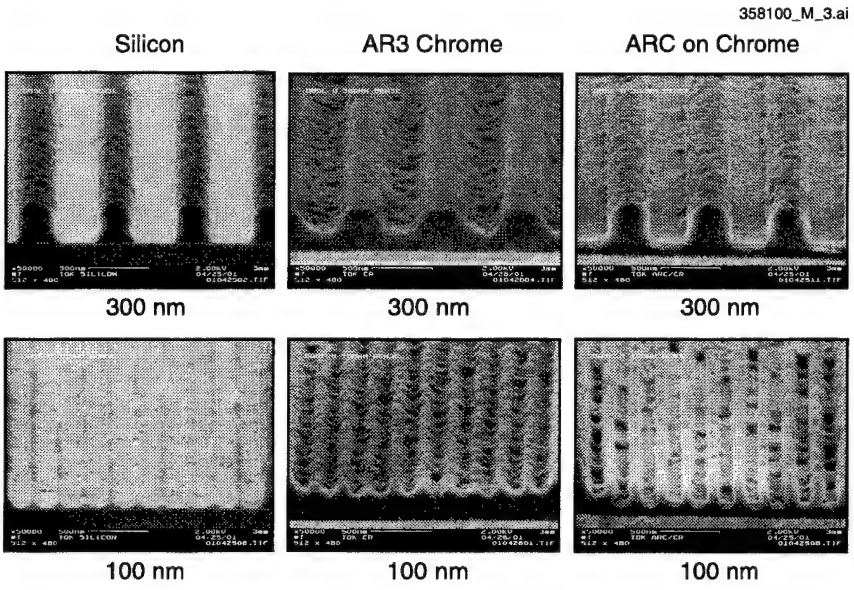

Figure 3-3. Imaging of 100- and 300-nm dense lines at 2.8 μC/cm^2 on OBER-CAP209-EL on silicon, AR3 chrome, and organic ARC on AR3. Substrate sensitivity, manifest as incomplete development on AR3 chrome, is not present on silicon or ARC.

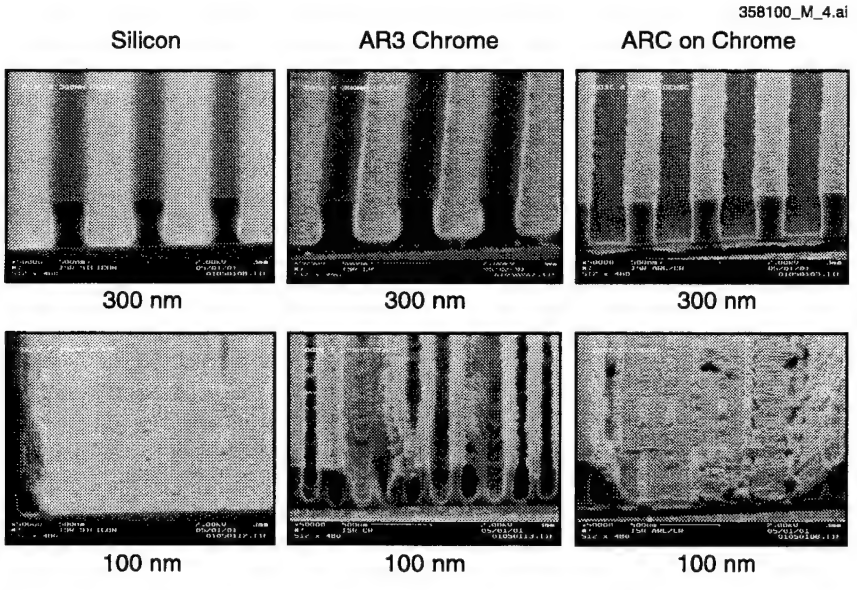

Figure 3-4. Imaging of 100- and 300-nm dense lines at 9.8 μC/cm^2 on TEBM 840 on silicon, AR3 chrome, and organic ARC on AR3. Substrate sensitivity, manifest as incomplete development on AR3 chrome, is not present on silicon or ARC.

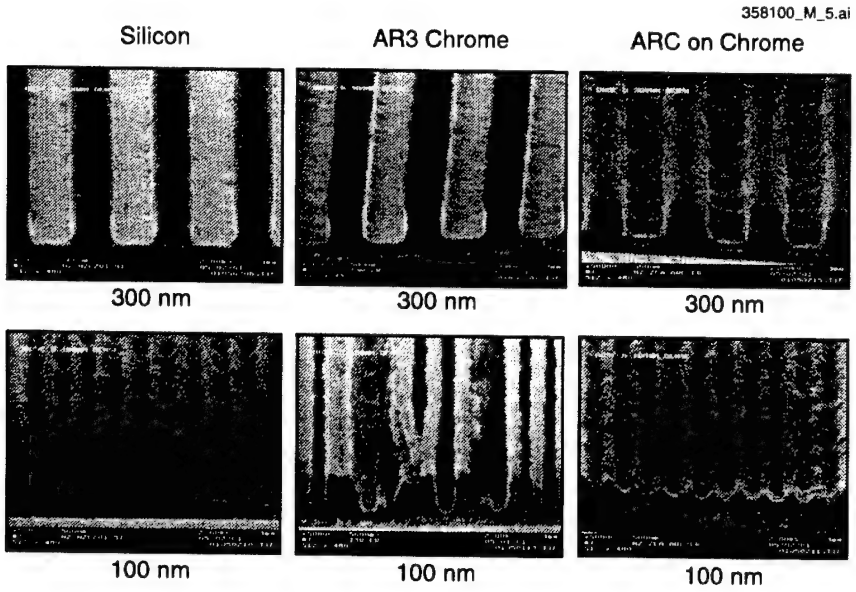

Figure 3-5. Imaging of 100- and 300-nm dense lines at 6.6 μC/cm^2 on ZCA-201 on silicon, AR3 chrome, and organic ARC on AR3. Substrate sensitivity, manifest as incomplete development, on AR3 chrome and ARC, is not present on silicon.

reduced resolution on Shipley AR3 is unexplained at this time, although it does indicate that the substrate sensitivity of CA resists can be different on different substrates. In addition to removing the resist footing, the AR3 organic layer also gave similar resist resolution to that of the silicon substrate, with the exception again being the ZCA-201.

This study has demonstrated that the AR3 chrome substrate can degrade the performance of CA resists. The cause is likely acid loss at the resist-substrate interface. Inserting an organic interlayer between the CA resist and the AR3 chrome can prevent the acid loss, and this was shown to be an effective means for reducing the degradation for most of the tested resists. It is also possible that a surface treatment of AR3 chrome or the use of other inorganic antireflective layers on chrome could reduce or eliminate the resist footing, although additional tests would be required to determine this.

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4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

4.1 STORAGE AND STIMULATION OF B CELLS

The CANARY (Cellular Analysis and Notification of Antigen Risks and Yields) detector is based on the B cell, an immune cell that expresses antibodies on its surface that bind to specific antigens, such as bacteria, viruses, or toxins. In the presence of large antigens, the binding of multiple antibodies on the surface of the B cell to the antigen generates a chemical cascade within the cell, resulting in an increase in the intracellular calcium concentration. In order to detect the intracellular calcium flux that occurs when the cells bind to antigen, the cells are also engineered to produce aequorin, an enzyme normally produced in luminescent jellyfish. In the presence of high calcium, aequorin catalyzes the oxidation of coelenterazine, which in turn emits a photon. This light emission is detectable using a photomultiplier tube. In summary, complex antigens on the cell exterior bind to antibodies on the surface of immune cells. This binding generates a calcium flux into the cell cytosol, which in turn stimulates aequorin to oxidize coelenterazine and emit detectable light. We have previously reported [1] the engineering of cell lines that express antibodies specific for *Francisella tularensis*, *Yersinia pestis* (Yp), foot-and-mouth disease virus, and Venezuelan equine encephalitis virus.

However, engineering the cells to recognize a specific agent is only the first step towards utilizing the cells as detectors. The cells must still undergo several preparative steps before they are ready to detect agent. In a process called loading, the cells are centrifuged and resuspended in media containing coelenterazine (this aequorin substrate is membrane permeable and binds to aequorin in the cell cytoplasm). At the end of the loading step, the cells are washed of excess coelenterazine by multiple rounds of centrifugation and resuspension in fresh medium, and then allowed to recover for several hours. The cells are now ready to detect agent by using the hardware and methodology that we have previously described [1].

One of the challenges in fielding a cell-based assay system is the potential for interassay variation. One method of minimizing differences between individual assays is to perform as many of the required preparatory steps as possible on a large scale under well-controlled conditions, and to reduce the number of steps required in numerous, small-scale devices in the field. The cells can be transported and stored frozen, but the goal is to freeze the cells at a point in their preparation so as to require very little processing between thawing the cells and assaying for the presence of agents. To this end the effects and methodologies of cell freezing on the CANARY assay are being examined.

An immediate and unsuspected benefit of using cells that are frozen and recently thawed is that the photon output from these cells in response to agent is both stronger, as shown in Figure 4-1, and more consistent. Control cells specific for Yp, loaded with coelenterazine and challenged with 500,000 killed Yp, gave a maximal response in this experiment of ~9500 photons per second. However, cells that were frozen and thawed 24 h prior to loading with coelenterazine showed a sixfold increase in signal over

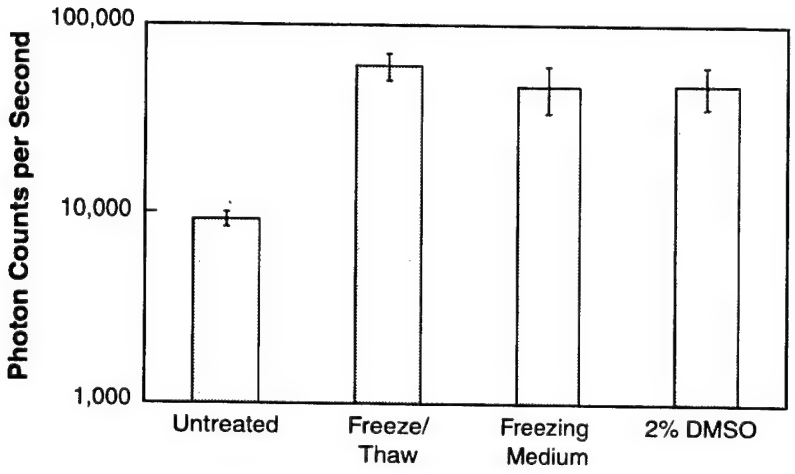

Figure 4-1. Effects of cell treatments on the response of Yersinia pestis (Yp) specific B cells to killed Yp. Cells were challenged with 50 µl of 10,000,000 Yp/ml diluted in CO_2-I after various cell treatments. Untreated: Cells were grown in RPMI, loaded with coelenterazine, washed, recovered for 24 h, and challenged with Yp. Freeze/thaw: Cells were grown in RPMI, transferred to freezing medium, and frozen. Thawed cells (1 ml) were placed into 4 ml of RPMI and incubated at 37°C for 24 h, loaded with coelenterazine, washed, recovered for 24 h, and challenged. Freezing medium: Cells were grown in RPMI, transferred to freezing medium and incubated at room temperature for 10 min. Cells (1 ml) were placed into 4 ml of RPMI and incubated at 37°C for 24 h, loaded with coelenterazine, washed, recovered for 24 h, and challenged. 2% DMSO: Cells were grown in RPMI, transferred to RPMI containing 2% DMSO and incubated at 37°C for 24 h, loaded with coelenterazine, washed, recovered for 24 h, and challenged.

untreated cells. The gain in signal resulting from a freeze/thaw cycle can be reproduced by exposing the cells to freezing medium, without actually freezing the cells. It appears that at least the majority of this enhancement is induced by one component of the freezing medium, dimethyl sulfoxide (DMSO), which alone can stimulate the cells to a similar degree as a complete freeze/thaw cycle. The fact that cells can be frozen is well known and widely used in biological research, but the fact that the CANARY cell response to agent can be stimulated by freezing, or by treatment with DMSO, is an unexpected benefit of this long-term storage method.

The ability to freeze cells would allow the production of large numbers of cells at a central site, where they can be well characterized, frozen, and shipped when and where they are needed. However, this still leaves the processes of thawing, recovery (several hours), loading with coelenterazine (1–2 h), washing and recovery (several hours) to be carried out in the field. We therefore attempted to bypass as many of these steps as possible prior to freezing. Cells were treated with DMSO, washed, loaded with coelenterazine, washed and recovered, and then frozen. Upon thawing, the cells were washed once and tested within 1 h using 50 μl of agent at the indicated concentrations, shown in Figure 4-2. The limit of detection using these cells was 10^4 Yp/ml (500 Yp total), about one order of magnitude less sensitive than the limit of detection for cells generated in the traditional manner.

A complementary scheme by which handling requirements can be minimized is to extend the time over which a given set of cells remains active after thawing. Longevity experiments on cells loaded before freezing are in the early stages, but with minimal optimization a moderate response can be attained after 4 days at room temperature, as seen in Figure 4-3. At this time point, the signal from Yp at 10^4/ml is nearing background levels, but still discernible in this particular experiment. This provides a reasonably wide window (<1 h to 4 days) during which a given aliquot of cells can effectively be used to assay for the presence of biological agents. It remains to be determined how long these coelenterazine-loaded cells can be frozen, and whether this method of cell preparation actually improves interassay variation. Attempts are under way to extend the functional life of charged cells at room temperature and to explore different methods of long-term storage.

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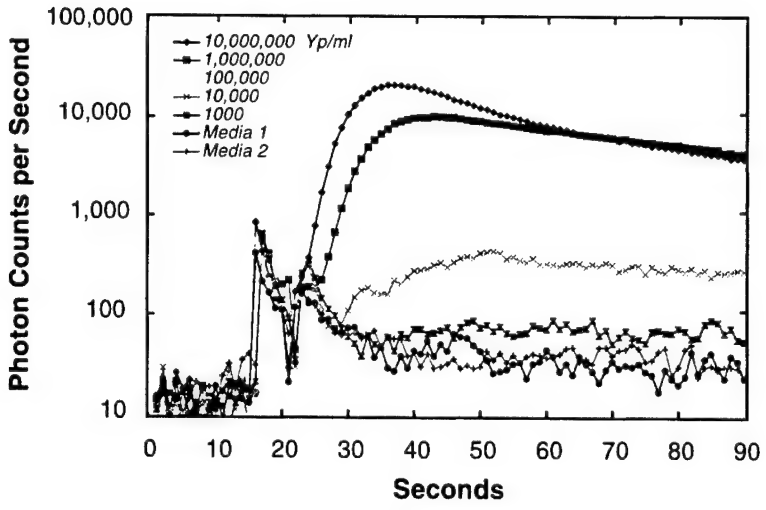

Figure 4-2. Response of Yp-specific cells charged with coelenterazine prior to freezing, with ~1-h post-thaw. Yp cells were grown in RPMI media to a concentration of ~500,000/ml. Cells were counted, centrifuged, and resuspended in RPMI containing 2% dimethyl sulfoxide and incubated overnight at 37°C. Cells were counted, centrifuged, and resuspended in CO_2-I media containing coelenterazine and incubated at room temperature in the dark for 2 h. Cells were washed with CO_2-I media and placed on a rotator overnight at room temperature. Cells were centrifuged, resuspended in CO_2-I media containing 10% DMSO and additional 10% fetal bovine serum, frozen at –80°C, and transferred to liquid nitrogen the following day. Cells were thawed, diluted in 10 ml of CO_2-I media, centrifuged, resuspended in CO_2-I at a concentration of 500,000 cells/ml, and assayed using 50 µl of killed Yp diluted to the indicated concentrations in CO_2-I media.

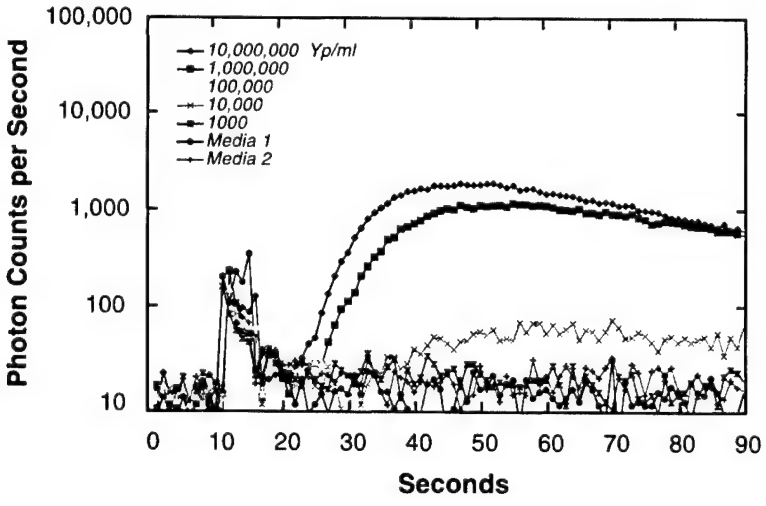

Figure 4-3. Response of Yp-specific cells charged with coelenterazine prior to freezing, with four days post-thaw. The same cells as those used in Figure 4-2 were assayed after incubation for four days at room temperature using 50 µl of killed Yp diluted to the indicated concentrations in CO_2-I media.

5. ADVANCED IMAGING TECHNOLOGY

5.1 SIMULATED TRANSIENT ANALYSIS OF AN ELECTRONICALLY SHUTTERED CHARGE-COUPLED DEVICE IMAGER

A variety of interesting two-dimensional imaging applications require multiple sequential image acquisitions at frame times in the submicrosecond to subnanosecond range. A 512×512-pixel, multiframe charge-coupled device (CCD) imager capable of collecting four sequential image frames at megahertz rates has been demonstrated [1]. To operate at fast frame rates with high sensitivity, the imager uses the electronic shutter technology that was developed for back-illuminated CCD imagers [2]. In this context, it is of considerable interest to explore the limits imposed by the electronic shutter for high-speed imaging. In this investigation, we report the results of a transient analysis performed using the device simulator ATLAS to analyze the electronic shutter switching characteristics.

Figures 5-1 and 5-2 illustrate the operational features of the electronic shutter for various gate electrode biases; details of the electronic shutter structure, fabrication, and operation are given in [2]. Figures 5-1(a) through 5-1(c) display hole concentration contours under the (12 μm wide) gate of a CCD structure obtained from the two-dimensional steady-state solution where the applied electrode bias is 4, 7, and 12 V, respectively. The electronic shutter in the device cross section shown is characterized by a region of high concentration of p-type dopant (p buried layer) formed approximately 2 μm below the wafer surface (yellow region in the figure). For a gate bias of 4 V, the holes in the p buried layer remain intact and the depletion region is confined to the area between the silicon-to-silicon-dioxide interface and the p buried layer. At 7-V bias, the depletion region begins to "punch through" the p buried layer. Above 7 V, the depletion region expands deep into the substrate. For example, at a 12-V bias, the depletion extent has nearly reached the back-side wafer surface.

Figure 5-2 illustrates the corresponding simulated electric potential as a function of depth along a vertical line in the middle of the device from the silicon-to-silicon-dioxide surface to the wafer back side for the three selected bias conditions of Figure 5-1. From the 4-V curve, it is apparent that when the p buried region is undepleted, a potential barrier to electron flow of ~200 mV is observed. At 7 V, this barrier is removed and the shutter is "open" or in the punch-through state. Note that for both the 4- and 7-V cases, a large charge-neutral substrate region exists where the voltage drop across the substrate is essentially zero or very low. Photoelectrons generated in this charge-neutral region diffuse relatively slowly until entering the depletion region where the electric field can accelerate the carriers into the CCD buried channel. Additionally, only for voltages greater than 7 V, where the barrier has been removed, would collection take place efficiently. For the 12-V case, where the depletion region extends to the back-side surface, a large potential variation with depth is formed which results in rapid charge collection indicative of a high electric field.

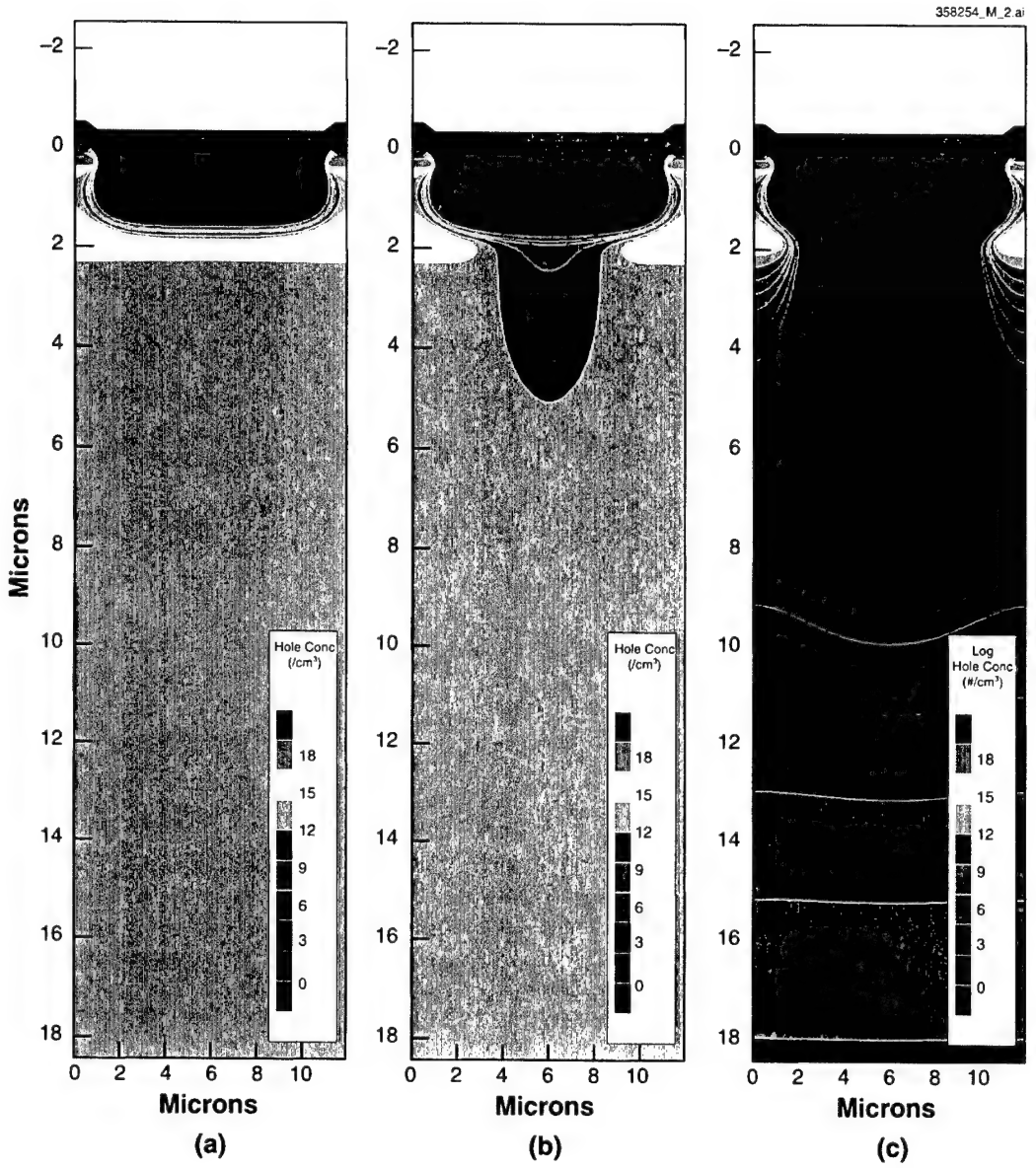

Figure 5-1. Simulated hole concentration contours obtained for electronically shuttered device with gate electrode applied bias of (a) 4, (b) 7, and (c) 12 V.

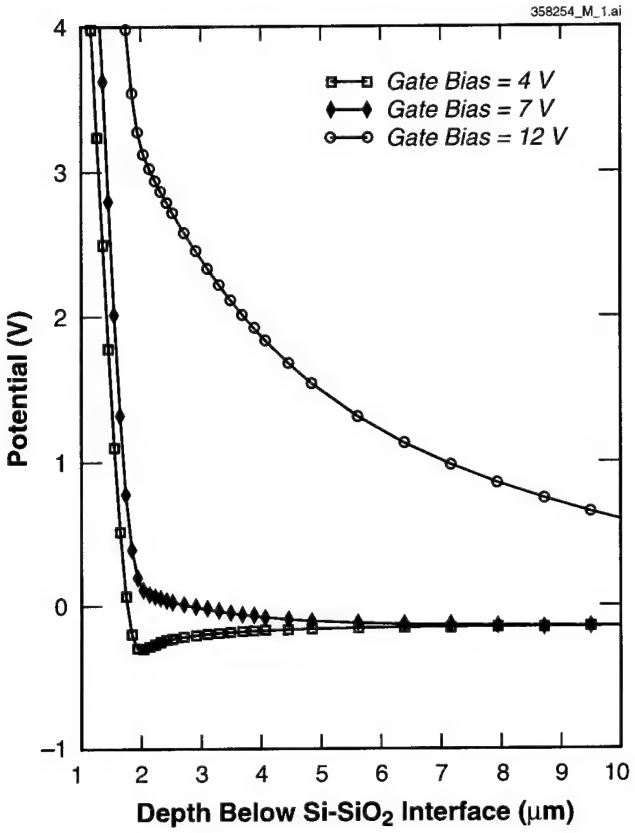

Figure 5-2. Electric potential as a function of depth along vertical line in middle of device structure and for the selected biases indicated in Figure 5-1.

In the remainder of this section, the transient electronic shutter response is investigated for fast CCD gate voltage pulses. Figure 5-3 gives composite hole contour plots for nanosecond-scale applied CCD gate voltages. It has been observed that an electric field is created across the neutral substrate that accelerates the photoelectrons towards the CCD buried-channel collection region before the depletion region forms in the substrate.

In the present analysis, a linear voltage ramp from 4 to 25 V was applied to the gate electrode with a ramp time of 1 ns to "open" the shutter. This was followed with no delay by a subsequent ramp from 25 to 4 V in 1 ns to "close" the shutter. Figures 5-3(a) and 5-3(b) display the hole concentration contours, for the same structure used in Figure 5-1, at the 1-ns open and close shutter-state intervals, respectively. What is apparent in both cases is that the holes in the substrate do not respond to the applied bias in subnanosecond times and the depletion region extent remains limited. However, the holes in the middle of the *p* buried

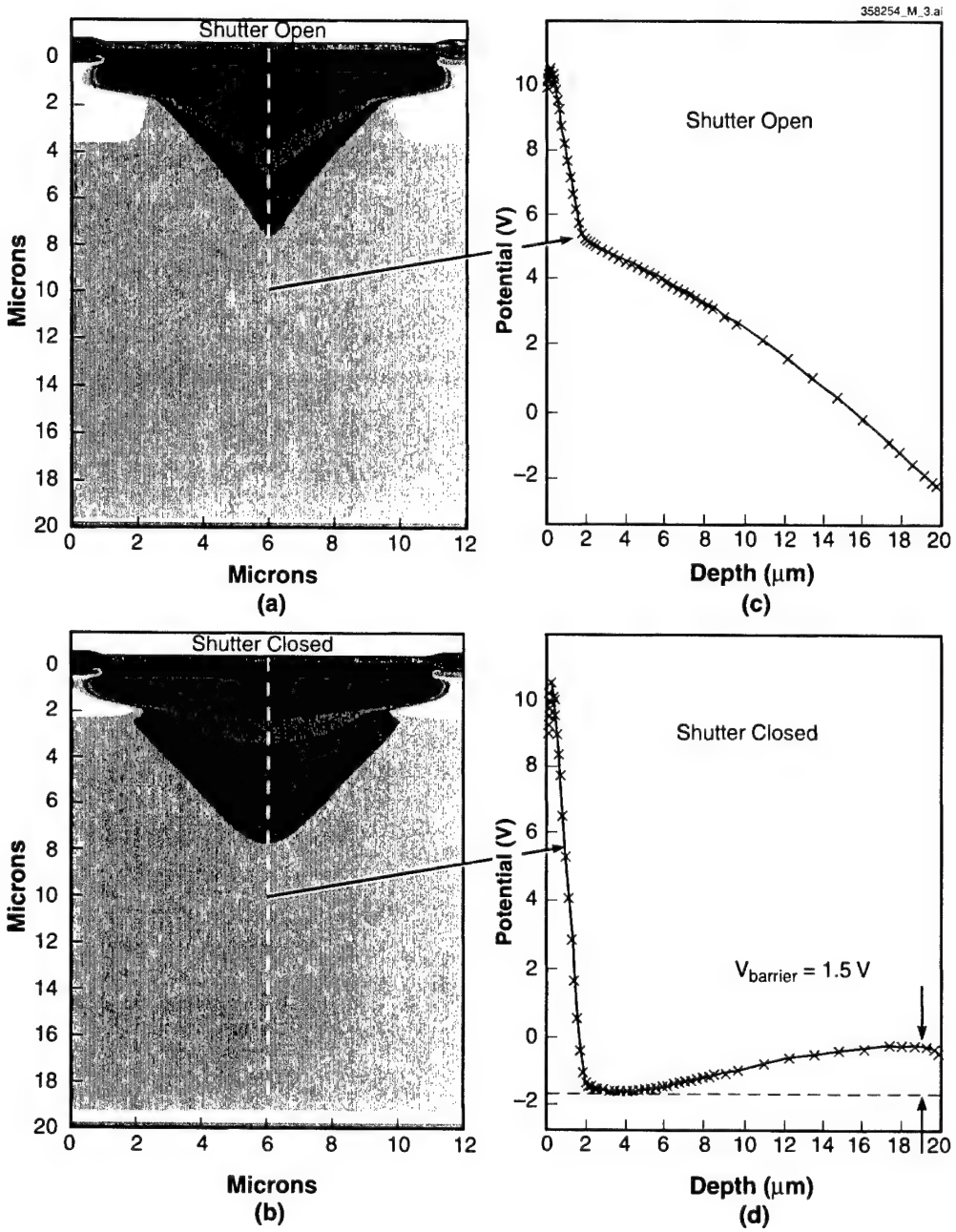

Figure 5-3. (a) Hole concentration contours obtained from transient solution where the gate electrode is pulsed from 4 to 25 V in 1 ns (shutter-open operation). (b) Hole concentration contours obtained from transient solution where the gate electrode was subsequently pulsed from 25 to 4 V in 1 ns (shutter-close operation). (c) Potential vs depth for the corresponding shutter-open operation. (d) Potential vs depth for the corresponding shutter-close operation.

layer are depleted. Even when the bias is returned to 4 V, the holes do not respond quickly enough to restore the original *p* buried layer.

However, as shown in the companion plot of the potential in Figure 5-3(c), when a high bias is applied in subnanosecond time frames, a large electric field, indicated by a large variation in potential with depth, is immediately formed across the neutral substrate region. This is in stark contrast to what is observed for the steady-state solution illustrated in Figure 5-2 where the electric field in the substrate is very low. As long as the shutter potential barrier is removed or punched through, very fast collection of photogenerated charge would be expected until this high field relaxes to the steady state value. While the holes do not respond to the fast voltage pulse to form a deep depletion region, most of the ramped gate voltage must be dropped across the neutral substrate.

When the shutter is pulsed to the close state by ramping the applied bias from 25 to 4 V, an equally interesting result is observed as displayed in the corresponding potential vs depth plot of Figure 5-3(d). Although the *p* buried layer is not fully reconstituted in nanosecond-time frames, as mentioned above, a negative space charge region from the depleted *p* buried layer creates a large potential barrier to electron flow which effectively closes the shutter. Note that this barrier is considerably higher in magnitude (1.5 V) than the shutter barrier in steady state at the instant the gate bias reaches 4 V. Thus, shutter-close operation is nearly instantaneous (20 μm divided by the speed of light in silicon is approximately 0.2 ps) and will be limited in speed by the ability to deliver a pulse to the gate electrode.

In summary, transient simulations done for nanosecond switching voltages show that the shutter is dynamically opened and closed in nanosecond times. When the shutter is opened, photoelectrons are collected by an electric field in the neutral substrate even though a depletion region has not formed. The photoelectrons are collected in approximately a nanosecond while the steady state depletion region does not form for tens of nanoseconds. Further, lowering the applied voltage creates a volt-level barrier in fractions of a nanosecond, effectively closing the shutter very efficiently and quickly. Holes eventually return to the *p* buried region reducing the barrier to a few hundred millivolts, but it is still sufficient to repel photoelectrons from the CCD collection channel.

In the dynamic regime, charge collection will proceed in nanosecond time frames and will be limited by the extent of the lateral fields in the device, the separation of the collecting electrodes, and the ability to get the voltage pulse to the pixel.

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6. ANALOG DEVICE TECHNOLOGY

6.1 CHARGE-DOMAIN ANALOG-TO-DIGITAL CONVERTER FOR A CHARGE-COUPLED DEVICE IMAGER FOCAL PLANE

A previous report [1] described a silicon process technology for integrating a high-performance charge-coupled device (CCD) imager with an on-focal-plane analog-to-digital (A/D) converter (ADC). This technology provides for the simultaneous fabrication of 0.35-μm silicon-on-insulator (SOI) CMOS devices with high-performance CCDs in the underlying "handle" wafer. The work cited described a 128 × 128-pixel imager integrated with a charge-domain ADC and on-chip circuitry for clocking the CCD imager gates. The resulting integrated imager functioned correctly, but the performance of the ADCs was very limited (about 3 bits of effective resolution).

A second-generation design has been completed, using the same process and incorporating the same basic functionality, but targeting much higher performance. The CCD imaging array was expanded to 640 × 960 pixels, and the clock circuitry was enhanced to drive this relatively high capacitance array at a 10-Mpixel/s rate. The ADC was completely redesigned, with a targeted resolution of 12 bits, sample rate of 10 megasamples per second, and power dissipation of ~10 mW. The present section provides some details of the ADC design.

The ouput signal from the CCD imager is a series of charge packets, with the quantity of charge (electrons) in each packet proportional to the number of photons integrated in a single pixel. In this design, the targeted full-pixel charge was 100,000 electrons, or 16 fC. The design goal for the ADC was to quantize this charge to 12 bits of resolution; this goal corresponds to a least-significant bit (LSB) of ~25 electrons. In an ideal ADC, the corresponding quantization noise would be ~7 electrons.

We considered various approaches to this rather daunting goal. In the planned ADC architecture, the signals remain in the charge domain throughout the A/D conversion process. An early idea was to perform charge-domain amplification on the direct imager-output charge packets before A/D conversion, thereby alleviating the ADC's charge-resolution requirements. Performing this amplification without adding unacceptable noise did not, however, appear feasible. In the end, we decided to attempt the direct A/D conversion of the unamplified pixel charges.

One important consideration that eases the difficulty of this task is the fact that the pixel-charge signals are shot noise limited: the pixel charges have a built-in noise equal to the square root of the charge (in electrons). For the 100,000-electron full scale, for example, the shot noise is ~320 electrons. Quantizing this signal to only 8 bits is sufficient to make quantization noise insignificant compared to the shot noise. For smaller pixel charges, the ratio of shot noise to pixel charge is even lower, so fewer bits are required, although the required charge resolution is smaller. This situation is depicted in Figure 6-1, which also shows that a 12-bit ADC has quantization noise that is completely negligible compared to shot noise for all but the smallest pixel charges (less than 100 electrons or so).

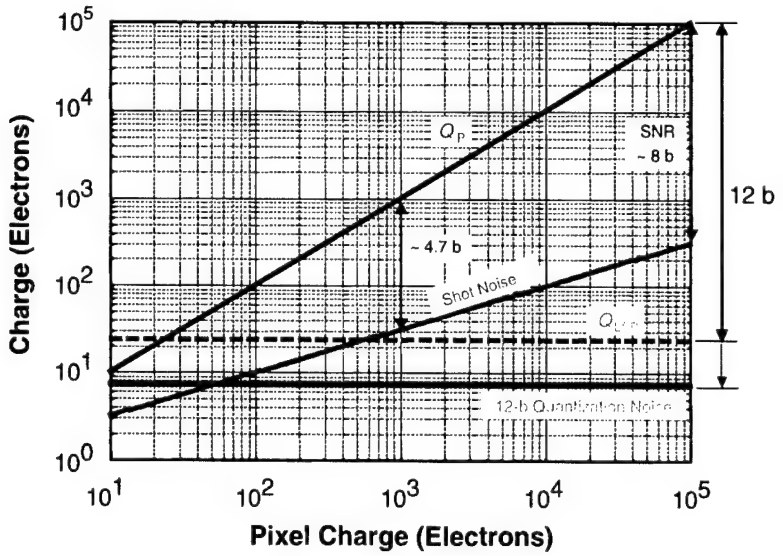

Figure 6-1. Imager dynamic range showing the pixel charge Q_P and the corresponding shot noise (equal to $\sqrt{Q_P}$). The signal-to-noise ratio (SNR) for a full-scale pixel is 320:1, ~8 effective bits. For comparison, the SNR of a pixel with 1% of full-scale charge (1000 electrons) is only 32:1, less than 5 effective bits. The quantization noise of a 12-bit quantizer with 100,000-electron full scale is ~7 electrons, equal to the shot noise of a 49-electron signal.

This observation led to the development of a floating-point-like A/D conversion approach, in which resolution for the largest signal values is 8 bits, with an LSB of ~400 electrons and a corresponding quantization noise of ~90 electrons. Smaller pixel charges are resolved to fewer bits, but with smaller LSBs, such that the quantization noise is always substantially less than the shot noise. The smallest pixel charges are resolved with an LSB of 25 electrons (quantization noise of 7 electrons) as would be the case with an ordinary 12-bit ADC. This scheme, which we call a sliding-scale ADC, is depicted in Figure 6-2. The output data representation of a sliding-scale ADC is shown in Figure 6-3. As will become apparent below, sliding-scale encoding is the only practical way of meeting the charge-resolution requirement of this application.

The ADC architecture used in this work is based on the one described in [2], which implements a pipelined differential successive-approximation algorithm in the charge domain. In the present work, several modifications to the cited architecture were developed in order to accommodate the demanding charge-resolution requirements. The resulting design is single ended rather than differential, incorporates more sensitive charge-comparison methods, and handles adjustment (reference) charge in a way that supports sliding-scale encoding.

The ADC algorithm developed in this work can be understood with the aid of Figure 6-4. This figure shows one pipeline stage of the ADC. The stage conveys three charge streams, each in a separate CCD shift

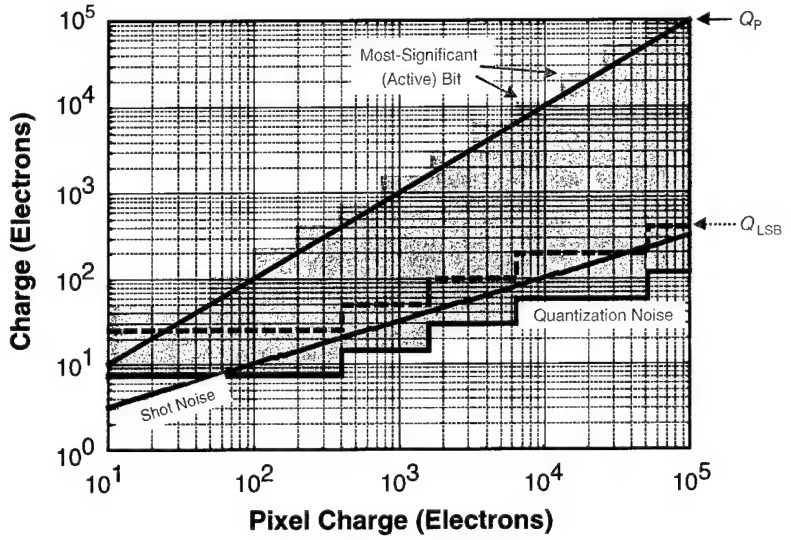

Figure 6-2. Sliding-scale analog-to-digital converter (ADC) dynamic range. The quantization noise is maintained below the pixel-charge shot noise down to a limiting value equivalent to 12-bit resolution with respect to full scale. The number of bits representing any charge is always sufficient to handle that charge's shot-noise-limited SNR.

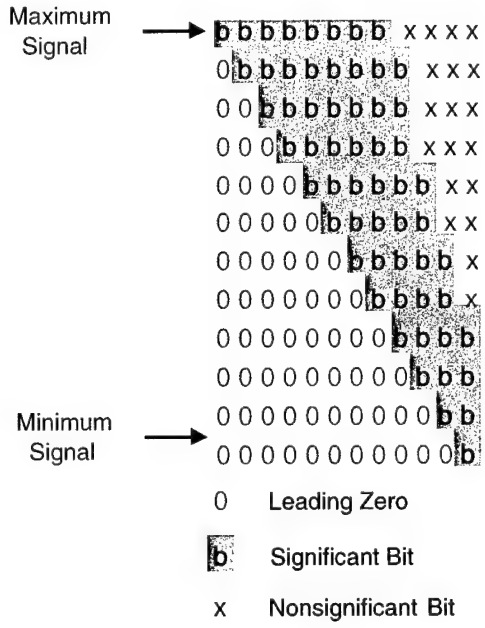

Figure 6-3. Sliding-scale data representation. The data output from the sliding-scale ADC is a constant 12 bits. For successively smaller signals, more leading bits are zeros, and more low-order bits become significant. Enough bits are significant for each signal value to adequately represent its shot-noise-limited SNR.

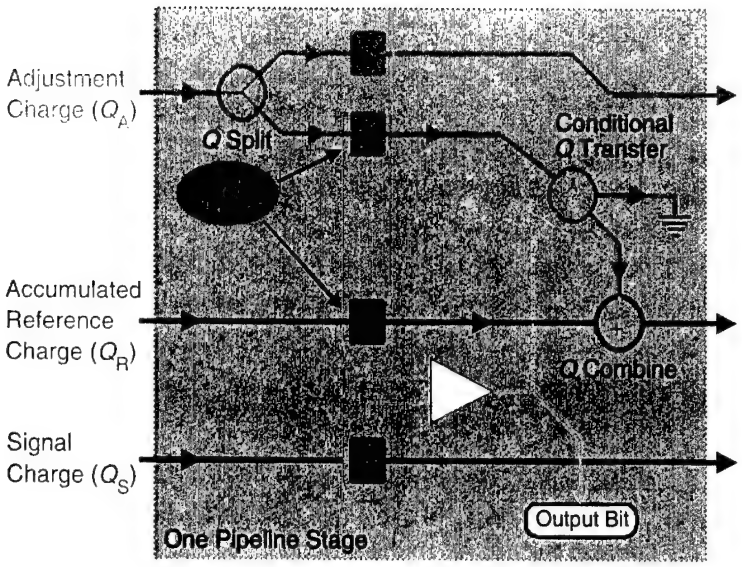

Figure 6-4. Charge-domain ADC algorithm. One stage of the pipeline is shown; charges enter from the left, are processed in the stage, and exit to the right. The colored rectangles represent charge storage, the heavy lines represent charge movement (charge-coupled device transfer), the circles represent other charge operations (splitting, conditional transfer, and merging), and the triangular "amplifier" symbol represents a comparator, which compares the signal charge Q_S to the "preview charge" $Q_A + Q_R$.

register: the signal charge Q_S, the accumulated reference charge Q_R, and the adjustment charge Q_A. Within the stage, the adjustment charge (derived from an initial reference charge) is split into two pieces, each half the size of the incoming packet. One piece is passed on to the next stage. The other is added to the incoming Q_R—without being irreversibly combined—to form a temporary "preview charge" $Q_R + Q_A/2$, and compared to Q_S. As a result of this comparison, Q_R is adjusted as follows before being passed on to the next stage:

$$Q_S \geq (Q_R + Q_A/2) \Rightarrow Q_{R(outgoing)} = Q_R + Q_A/2$$

$$Q_S < (Q_R + Q_A/2) \Rightarrow Q_{R(outgoing)} = Q_R$$

The conditional addition is accomplished, as shown in Figure 6-4, by transferring the half-Q_A charge packet conditionally to the "Q combine" block—where it is merged with Q_R—or to a charge drain (indicated by a "ground" symbol).

Note that the stage modifies Q_A in a deterministic way. Incoming Q_A is divided by two to produce the outgoing packet. Q_R is modified adaptively as indicated above, based on a comparison with the signal. The signal charge Q_S is not modified at all; it is passed unchanged to the next stage.

The values of Q_S, Q_R, and Q_A in a representative case are shown for the first six ADC stages in Figure 6-5. In the first ADC stage, $Q_R = 0$. After each stage, the outgoing Q_R packet has been driven closer

to Q_S, without overshooting it. Since the potential increment to Q_R in each stage (that is, $Q_A/2$) is half that in the previous stage, this algorithm generates a binary-coded representation of the input signal. This ADC can thus be seen as a charge-domain implementation of the standard successive approximation algorithm widely used for A/D conversion.

This algorithm has a particular advantage for the present application. Because the signal charge passes through each stage without modification, and because the reference charge is not incremented from zero until the increment is less than the signal charge, *no adjustment charge packet larger than the signal charge is ever irreversibly introduced into the A/D conversion.* Larger adjustment packets have unavoidable noise components that would dominate the noise of small signal packets; since these early adjustment packets, corresponding to leading zeros in the sliding-scale data format, are discarded in this algorithm, their noise does not corrupt the ADC results.

If the incoming full-scale charge could be chosen to be as large as needed, then the noise of early (more significant) bits would not be an issue, and an ordinary 12-bit ADC could be employed. Given the limited full-scale signal (which is set by the imager pixel size), however, this condition is not met. Therefore, in order to convert the entire pixel-charge range, some type of auto-ranging is needed; the sliding-scale method incorporates this requirement directly into the ADC algorithm.

Implementation of this algorithm in silicon was quite direct in the design reported here. The operations of charge splitting, storage, merging, and conditional and unconditional transfer are carried out in the charge domain using CCD methods. Nondestructive charge-to-voltage conversion for comparison is accomplished using floating CCD gates. Only the comparison operation requires conventional circuitry, a voltage comparator.

One additional technique was adopted to enhance resolution. The Q_S and Q_R streams were interleaved in a single CCD register, rather than carried in two separate registers as shown in Figure 6-4. This arrangement allows the charge comparison to be performed *sequentially* rather than in parallel as in [2]. This sequential comparison is equivalent to the correlated-double-sampling charge sensing often employed in CCD imagers; it rejects $1/f$ comparison noise and eliminates layout mismatch and comparator offset voltage as comparison error sources. The required doubling of CCD clock rate is not a problem in the technology used.

The SOI-CMOS process presented certain difficulties, as well as some advantages, in the implementation of the voltage comparators. Hot electrons in SOI metal-oxide semiconductor field-effect transistors (MOSFETs) can cause threshold shifts of several hundred millivolts, because of charging of the floating body. Such threshold shifts would be catastrophic in the present design, where resolution of several hundred *micro*volts is required. In this design, we employed cascodes extensively to avoid the high V_{ds} values which produce hot electrons. In addition, we used source-body ties or H-gate structures in all critical devices, to minimize body-charge accumulation.

The low thermal conductance of SiO_2 leads to significant temperature rise in SOI field-effect transistors, even with the relatively low power employed, a few hundred microwatts at most in any one

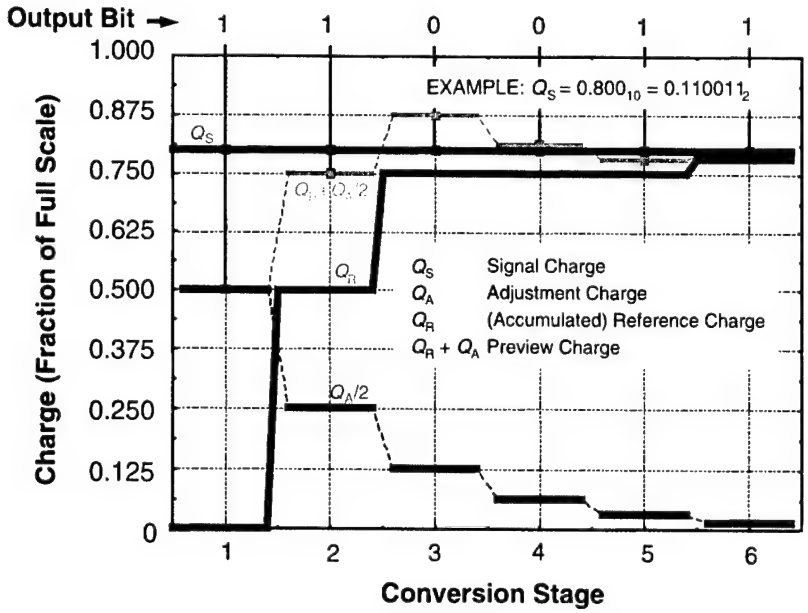

Figure 6-5. Charge-domain ADC algorithm. Values of Q_S, Q_A, and Q_R as well as the preview charge ($Q_A + Q_R$) are shown for the first six pipeline stages, for a representative input. Q_R approaches Q_S by successively smaller steps, without ever surpassing it. Unused Q_A packets, corresponding to zeros in the output word, are discarded and do not contribute to Q_R.

device. This effect can cause threshold offset between members of a differential pair, producing a history dependence of comparison results; we mitigated this effect to the extent possible by arranging to have all critical differential pairs share silicon islands and by minimizing power dissipation in such devices. On the other hand, the low power-delay product and small body effect of the SOI devices was used to advantage in minimizing the power of the comparator circuitry.

Based on analysis and SPICE simulation, we found that the resolution of this ADC is limited by two factors: voltage noise in the comparators and charge noise in the adjustment charges. The resulting conversion noise and its components are shown in Figure 6-6. The ideal quantization noise from Figure 6-2 is shown for reference. The ADC noise contribution is below the pixel shot noise down to ~1% of full scale. For smaller pixel-charge values, ADC noise rises to about 3× the shot noise. The limiting noise level for small pixel charges is ~18 electrons rms, with the excess noise dominated by the comparators. This ADC performance is equivalent to a signal-to-noise ratio of ~10.5 effective bits.

As is usual in such projects, we discovered various means of improving the performance of the ADC in the course of designing it. Also as usual, time was insufficient to permit incorporation of these

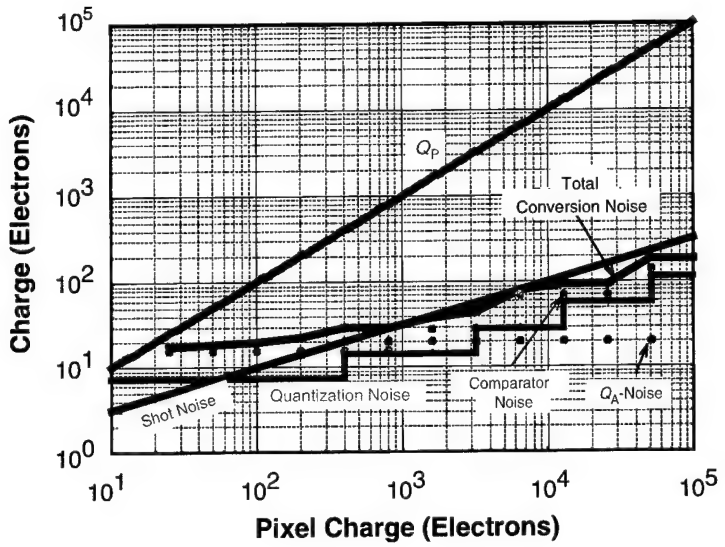

Figure 6-6. Simulated ADC performance. Pixel-charge and shot noise lines are the same as those in Figures 6-1 and 6-2, and the ideal quantization noise from Figure 6-2 is shown for reference. The principal noise sources—comparator noise and adjustment-charge noise—are shown, as well as the total conversion noise.

improvements in this design pass. Our catalog of potential improvements, all straightforward and with high probability of success, together should yield resolution of approximately *one* electron rms in a future design.

In summary, we have completed the design of a fully integrated ADC on a CCD focal plane, along with all necessary control and clock circuitry and CCD gate drivers. The simulated dynamic range is ~10.5 effective bits, with pixel charge resolution of ~18 photoelectrons. The output rate is 10 Mpixels/s, i.e., 30 frames/s for a videographics array (VGA) image format, and the power dissipation of the ADC is ~10 mW. The entire chip including imager is expected to dissipate ~25 mW.

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7. ADVANCED SILICON TECHNOLOGY

7.1 HIGH-PERFORMANCE FULLY DEPLETED SILICON-ON-INSULATOR RF CMOS

Silicon-on-insulator (SOI) CMOS offers many advantages over the bulk Si, such as reduced parasitic capacitance, suppressed short-channel effect, and simplified process. The floating-body effect associated with the SOI can be minimized by reducing the SOI thickness so that the channel region is fully depleted in normal operation. With its simple process and high packing density, the high-speed low-power fully depleted SOI (FDSOI) [1] is ideal for CMOS system-on-a-chip integration. Although cutoff frequency f_T as high as 85 GHz has been reported for a 0.15-μm FDSOI n-type metal oxide semiconductor field-effect transistor (MOSFET) [2], similar results on the maximum frequency of oscillation, f_{max}, and noise figure, parameters more relevant for rf circuits, have not been achieved. The main reason, suffered by all Si MOSFETs, is the high resistance of a deep-submicron gate. Here, we report the process of overlaying a metal strap on the poly-Si gate to lower the gate resistance. The resulting FDSOI CMOS with this T-gate structure has been characterized and it shows state-of-the-art rf performance.

The fabrication process is standard for digital FDSOI CMOS with self-aligned Co-silicide contacts [2]. The SOI layer on top of a 190-nm-thick buried-oxide (BOX) layer was thinned to a thickness of 45 nm. The length of the poly-Si gate and the thickness of the gate oxide are 0.2 μm and 4 nm, respectively. As shown in Figures 7-1(a) and 7-1(b), after the deposition and planarization by chemical-mechanical polishing (CMP) of the first oxide interlayer, the contact holes were etched to the source/drain silicide. Next, a slot is opened to expose the top of the entire poly-Si gate with an additional lithographic and timed-etch step, shown in Figure 7-1(c). Then, standard plug metal-fill/CMP followed by the first-level metal deposition and patterning completes the T-gate formation, as depicted in Figures 7-1(d) and 7-1(e). After that, the fabrication is completed with standard CMOS backend process.

A scanning electron micrograph (SEM) of the T-gate structure, consisting of TiN-Al plug fill and first-level interconnect metal, is shown in Figure 7-2. The width at the top of the T is 1.5 μm and the thickness of the plug metal as well as metal 1 is 0.6 μm. The sheet resistance of the silicide and the metal 1 are approximately 20.0 and 0.1 Ω/square, respectively. The maximum transconductance g_m at 1.5 V of drain bias is 340 μS/μm for an n-MOSFET and 225 μS/μm for a p-MOSFET. The maximum drain current I_{ds} are 370 and 310 μA/μm for the n- and p-MOSFET, respectively. Although the spacing of the source/drain contacts for T-gate MOSFETs has to be wider to satisfy the design rules, the resulting increase in series resistance is estimated to be less than 3%. The relatively low I_{ds} for the n-MOSFET is the result of low doping concentration in the extension regions, and an I_{ds} over 500 μA/μm has been achieved in our recent fabrication runs with improved implant schedules.

S parameters were measured with a network analyzer up to 50 GHz using microwave wafer probes. Measured f_T and f_{max} are plotted in Figure 7-3 for MOSFETs with two gate fingers and various finger

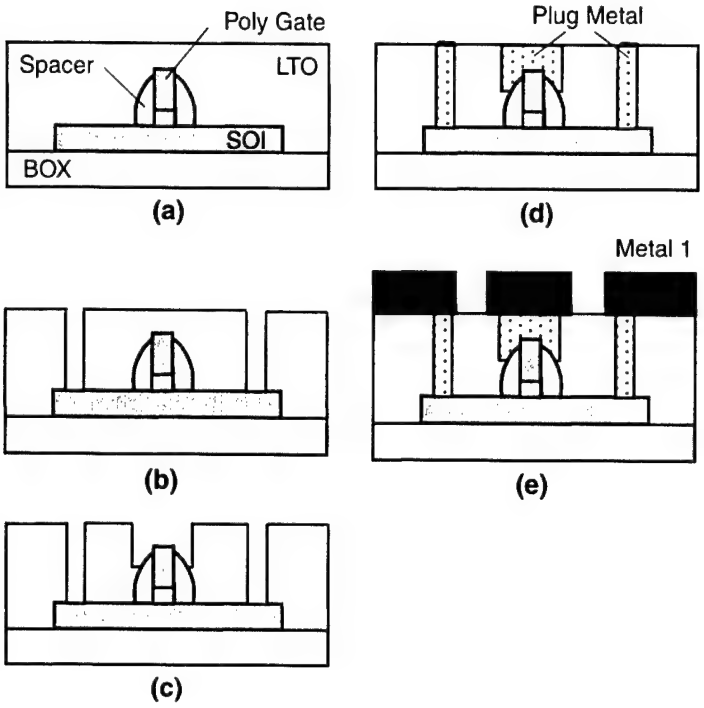

Figure 7-1. Process steps for T-gate formation: (a) Planarized oxide layer, (b) contact etch, (c) T-gate slot etch, (d) plug metal fill and chemical-mechanical planarization, and (e) metal-1 patterning.

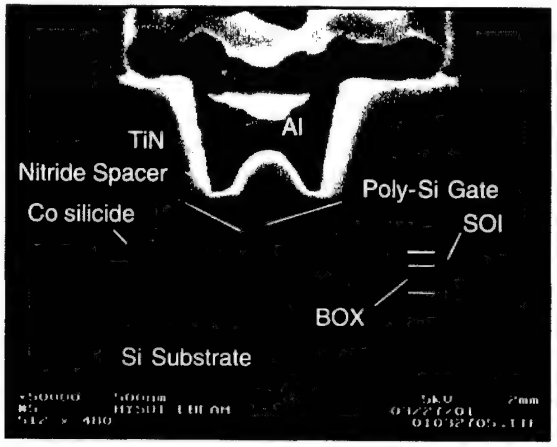

Figure 7-2. Cross-sectional view of fully depleted silicon-on-insulator T-gate metal oxide semiconductor field-effect transistor (MOSFET).

widths. The f_T does not change much with the gate finger width, and the highest f_T is 67 GHz for the n-MOSFET and 47 GHz for the p-MOSFET, all with two 10-μm-wide fingers (denoted as a 2×10 device). For the same gate finger width, the f_T for MOSFETs with added T-gate structure is slightly lower than that with conventional silicided poly-Si gate only. This is probably caused by the increased parasitic capacitance of the T gate.

The effect of gate resistance becomes obvious when the f_{max} is compared. With standard silicided gate, the f_{max} of an n-MOSFET decreases from 40 GHz with 5-μm finger width to 13 GHz when the finger width increases to 20 μm, and the f_{max} is always lower than the f_T. The sharp drop of f_{max} with wider finger is the result of increase in gate resistance, estimated from S parameters to be 815 Ω for the standard silicided gate and 15 Ω for the T-gate. For comparison, measured f_{max} of the T-gate n-MOSFET with 20-μm-wide gate finger is 75 GHz, which is nearly sixfold higher than the 13 GHz for the same device without the T-gate. Notice that the f_{max} is always higher than the f_T for T-gate MOSFETs, a desirable result usually found only in bipolar transistors. Similar behavior was observed for p-MOSFETs, where the highest f_T is 47 GHz with 20-μm gate finger and the highest f_{max} is 59 GHz with the T-gate.

The f_T value of the n-MOSFET reported here is comparable to the best of bulk-Si devices [3]–[5], and the f_{max} of the T-gate n-MOSFET is among the highest for Si MOSFETs, including a 0.1-μm T-gate MOSFET with raised source/drain structure [4]. To the best of our knowledge, the 59-GHz f_{max} is the highest reported for a p-MOSFET. Although all our results discussed so far are at 1.5 V of V_{ds}, the same supply voltage used for low-power digital circuits made in this FDSOI technology, there is a wide bias range in which high f_{max} can be achieved. For example, the f_{max} increases to 76 GHz for the n-MOSFET and to 63 GHz for the p-MOSFET at $V_{ds} = 2$ V, and it still remains above 70 GHz for the n-MOSFET at V_{ds} as low as 1 V. The V_{gs} was kept at 1 V for all the measurements.

As shown in Figure 7-4 for a T-gate n- and p-MOSFET with two 20-μm-wide gate fingers, a low minimum noise figure NF_{min} can be obtained over a large bias range. At 2 GHz, the best NF_{min} is 1.6 dB for the n-MOSFET and 1.7 dB for the p-MOSFET. The increase in NF_{min} at low V_{gs} for the n-MOSFET is the result of decrease in gain at these bias conditions. The NF_{min} increases with frequency and it reaches 3.5 dB at 18 GHz for the n-MOSFET. For comparison, the NF_{min} of the same 2×20-μm n-MOSFET without the T-gate is ~2.5 dB higher at the same bias. All MOSFETs, with or without the T-gate, have similar dc characteristics and comparable f_T's which are derived from the short-circuit current gain excluding the effect of the gate resistance. Since the device layout and dimensions are exactly the same, the lower NF_{min} is therefore attributed primarily to the lower resistance of the T-gate.

Because of the diminishing contribution from the pad parasitic capacitance, the NF_{min} generally improves with increasing total gate width [5]. Figure 7-5 is a plot of the NF_{min} as a function of frequency for a T-gate n-MOSFET with six 50-μm-wide gate fingers. At 2 GHz, the NF_{min} is 0.4 dB, with 18 dB of associated gain, at $V_{ds} = 1.0$ V and $V_{gs} = 0.5$ V. The NF_{min} has improved by 1.2 dB when the gate width increases from 40 to 300 μm and it remains below 1 dB at 6 GHz.

The NF_{min} reported here is comparable to that of SiGe bipolar transistors with an f_T of 90 GHz [7] and is lower than MOSFETs with higher f_T [5],[6], including a bulk-Si T-gate MOSFET [4] as well as a

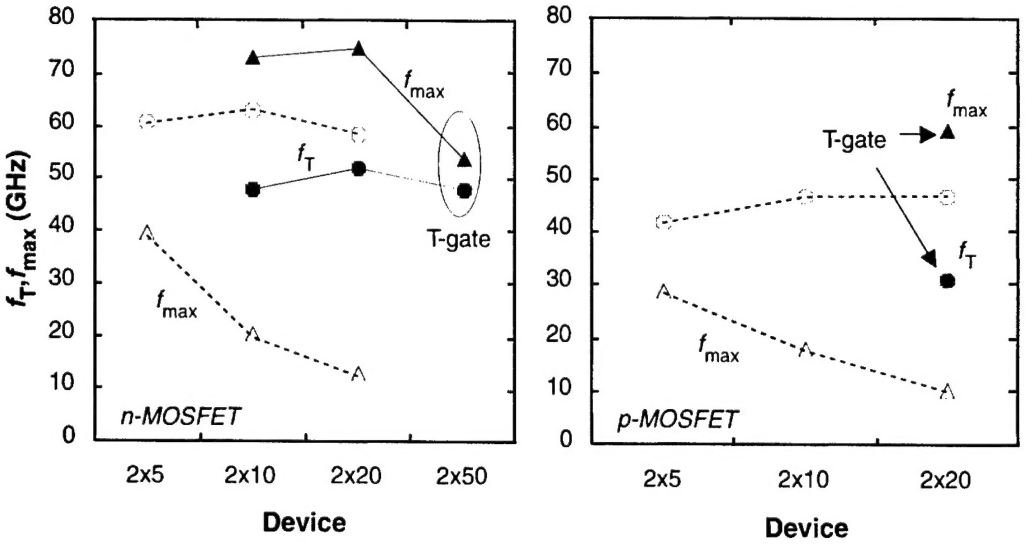

Figure 7-3. Measured f_T and f_{max} of n- and p-MOSFETs with various gate finger widths. The first digit refers to two gate fingers, and the second digit refers to finger width in micrometers. The drain and gate bias are 1.5 and 1.0 V, respectively. The dashed lines are devices without the Al overlay.

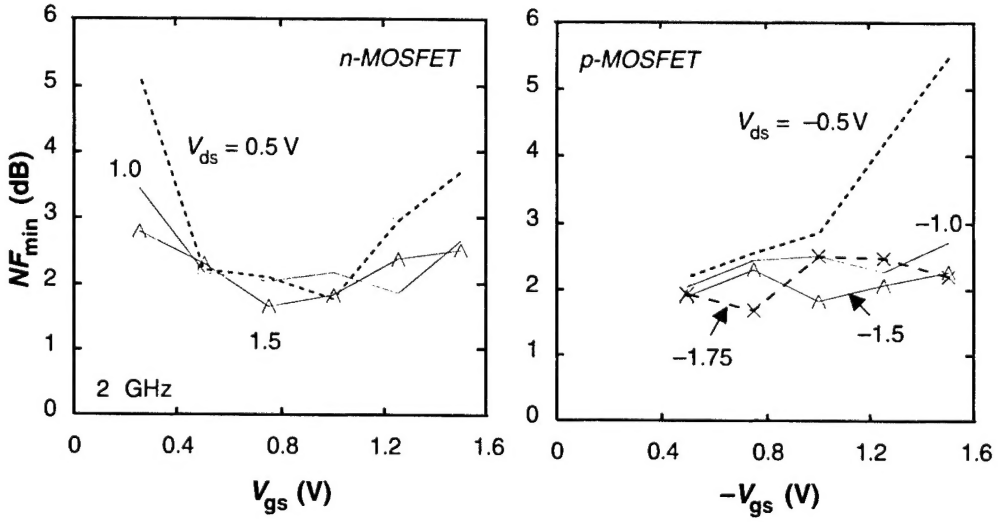

Figure 7-4. Measured NF_{min} of T-gate n- and p-MOSFETs with two 20-μm-wide gate fingers as a function of biases.

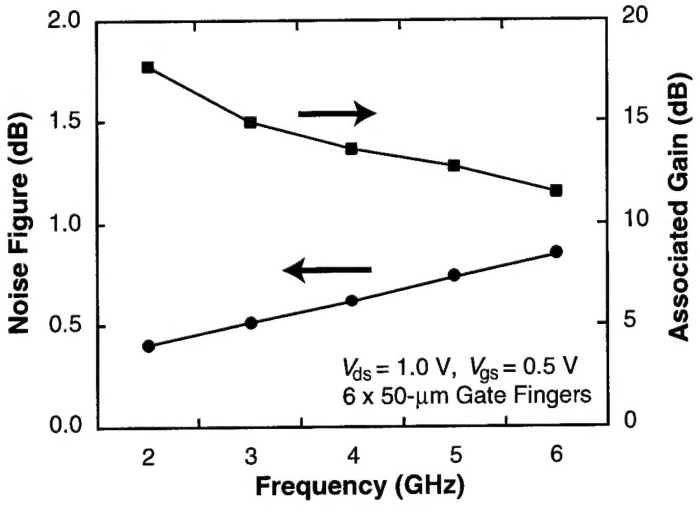

Figure 7-5. Measured NF_{min} and associated gain of T-gate n-MOSFET with six 50-μm-wide gate fingers.

0.1-μm-gate-length partially depleted SOI [8]. The noise power generated in our *n*-MOSFET, using the formula in [5], is –166 dBm/Hz, which is better than the –165 dBm/Hz for a GaAs metal semiconductor field-effect transistor and comparable to the –171 dBm/Hz for bulk-Si MOSFETs [5]. There has been concern about the noise property of SOI MOSFETs, especially for FDSOI having a very thin Si conduction channel sandwiched between two oxide layers. Although the low NF_{min} reported here is mainly the result of a low gate resistance, the noise-power calculation indicates that the FDSOI is not inherently inferior to bulk Si with respect to the noise performance.

The FDSOI CMOS for high-speed low-power digital circuits has been demonstrated in this work to have exceptional rf performance at the same low bias voltage. With added T-gate structure, the f_{max} and the noise figure are drastically improved so that in many instances they are superior to the best bulk-Si MOSFETs with a much shorter gate length. The low resistance of the T-gate allows the use of wide gate fingers without performance degradation, resulting in increased flexibility for laying out large MOSFETs that are commonly used in rf circuits. The rf performance can be further improved by optimizing the geometry and dimension of the T gate, such as increasing the metal thickness of the T or incorporating higher-level metallization for a wider T-top without violating the design rules for contact spacings.

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (*Leave blank*)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	15 February 2002	Quarterly Technical Report, 1 November 2001–31 January 2002

4. TITLE AND SUBTITLE

Solid State Research

5. FUNDING NUMBERS

C — F19628-00-C-0002

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Lincoln Laboratory, MIT
244 Wood Street
Lexington, MA 02420-9108

8. PERFORMING ORGANIZATION REPORT NUMBER

2002:1

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

HQ Air Force Materiel Command
AFMC/STSC
Wright-Patterson AFB, OH 45433-5001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

ESC-TR-2001-078

11. SUPPLEMENTARY NOTES

None

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (*Maximum 200 words*)

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 November 2001–31 January 2002. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, DARPA, MDA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

14. SUBJECT TERMS

quantum electronics
electro-optical devices
materials research
submicrometer technology
biosensor technology
molecular technology
advanced imaging technology
analog device technology
ytterbium fiber lasers
semiconductor lasers
electron-beam mask making
charge-coupled device imagers
analog-to-digital converters
silicon-on-insulator CMOS

15. NUMBER OF PAGES
68

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Same as Report	Same as Report	Same as Report